MILITARY STANDARD

TESTABILITY PROGRAM FOR ELECTRONIC SYSTEMS AND EQUIPMENTS

AMSC No. N3423

ATTS

DEPARTMENT OF DEFENSE
WASHINGTON, DC 20301

Testability Program for Electronic Systems and Equipments

MIL-STD-2165

1. This Military Standard is approved for use by all Departments and Agencies of the Department of Defense.

2.   Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Commander, Naval Electronic Systems Command (ELEX-8111), Washington, DC 20363-5100, by using the self-addressed standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

FOREWORD

1.   Testability addresses the extent to which a system or unit supports fault detection and fault isolation in a confident, timely and cost-effective manner. The incorporation of adequate testability, including built-in test (BIT), requires early and systematic management attention to testability requirements, design and measurement.

2.   This standard prescribes a uniform approach to testability program planning, establishment of testability (including BIT) requirements, testability analysis, prediction and evaluation, and preparation of testability documentation. Included are:

    a.   Testability program planning
    b.   Testability requirements
    c.   Testability design
    d.   Testability prediction
    e.   Testability demonstration
    f.   Testability data collection and analysis
    g.   Documentation of testability program
    h.   Testability review.

3.   This standard also prescribes the integration of these testability program requirements with other closely related, interdisciplinary program requirements, such as design engineering, maintainability and logistic support.

4.   Three appendices are included to augment the tasks of this standard:

    a.   Appendix A provides guidance in the selection and application of testability tasks.

    b.   Appendix B describes the Inherent Testability Assessment which provides a measure of testability early in the design phase.

    c.   Appendix C provides a Glossary of terms used in this standard.

CONTENTS

1. SCOPE

1.1 Purpose. This standard provides uniform procedures and methods for establishing a testability program, for assessing testability in designs and for integration of testability into the acquisition process for electronic systems and equipments.

1.2 Application. This standard is applicable to the development of electronic components, equipments, and systems for the Department of Defense. Appropriate tasks of this standard are to be applied during the Conceptual phase, Demonstration and Validation phase, Full Scale Development phase and Production phase of the system acquisition process.

1.3 Tailoring of tasks. Tasks described are intended to be tailored as appropriate to the particular needs of the system or equipment acquisition program. Application guidance and rationale for selecting and tailoring tasks are included in Appendix A.

2. REFERENCED DOCUMENTS

2.1 Issues of documents. The following documents, of the issue in effect on the date of invitation for bids or request for proposal, form a part of this standard to the extent specified herein.

STANDARDS

Military

MIL-STD-470	Maintainability Program for Systems and Equipment
MIL-STD-471	Maintainability Verification/Demonstration/Evaluation
MIL-STD-721	Definition of Effectiveness Terms for Reliability and Maintainability
MIL-STD-785	Reliability Program for Systems and Equipment Development and Production
MIL-STD-1309	Definition of Terms for Test, Measurement and Diagnostic Equipment
MIL-STD-1388-1	Logistic Support Analysis
MIL-STD-2077	Test Program Sets, General Requirements for

(Copies of standards required by contractors in connection with specific procurement functions should be obtained from the procuring activity or as directed by the contracting officer.)

3. DEFINITIONS AND ACRONYMS

3.1 Definitions. The definitions included in MIL-STD-1309 and MIL-STD-721 shall apply. In addition, the definitions of Appendix C are applicable.

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3.2 Acronyms and abbreviations. The following acronyms and abbreviations listed in this Military Standard are defined as follows:

a. ATE - automatic test equipment
b. ATLAS - abbreviated test language for all systems
c. BIT - built-in test
d. BITE - built-in test equipment
e. CDR - critical design review
f. CDRL - contract data requirements list
g. CFE - contractor furnished equipment
h. CI - configuration item
i. CND - cannot duplicate
j. DID - data item description
k. D&V - demonstration and validation
l. FMEA - failure modes and effects analysis
m. FQR - formal qualification review
n. FSD - full-scale development
o. GFE - government furnished equipment
p. GPETE - general purpose electronic test equipment
q. HITS - hierarchical interactive test simulator
r. ID - interface device
s. I/O - input or output
t. ILSMT - integrated logistic support management team
u. LSA - logistic support analysis
v. LSAR - logistic support analysis record
w. MTTR - mean time to repair
x. P/D - production and deployment
y. PDR - preliminary design review
z. R&M - reliability and maintainability
aa. ROM - read only memory
bb. SCOAP - sandia controllability observability analysis program
cc. SDR - system design review
dd. STAMP - system testability and maintenance program
ee. T&E - test and evaluation
ff. TPS - test program set
gg. TRD - test requirements document
hh. UUT - unit under test

4. GENERAL REQUIREMENTS

4.1 Scope of testability program. This standard is intended to impose and facilitate inter-disciplinary efforts required to develop testable systems and equipments. The testability program scope includes:

a. Support of and integration with maintainability design, including requirements for performance monitoring and corrective maintenance action at all levels of maintenance.
b. Support of integrated logistic support requirements, including the support and test equipment element and other logistic elements.

c.   Support of and integration with design engineering requirements, including the hierarchical development of testability designs from the piece part to the system.

4.2 Testability program requirements. A testability program shall be established which accomplishes the following general requirements:

a.   Preparation of a Testability Program Plan

b.   Establishment of sufficient, achievable, and affordable testability, built-in and off-line test requirements

c.   Integration of testability into equipments and systems during the design process in coordination with maintainability design process

d.   Evaluation of the extent to which the design meets testability requirements

e.   Inclusion of testability in the program review process.

4.3 Application of requirements. Detailed requirements described in this standard are to be selectively applied and are intended to be tailored, as required, and as appropriate to particular systems and equipment acquisition programs. Appendix A provides rationale and guidance for the selection and tailoring of testability program tasks.

5. DETAILED REQUIREMENTS

5.1 Task descriptions. Individual task requirements are provided for the establishment of a testability program for electronic system and equipment acquisition. The tasks are categorized as follows:

TASK SECTION 100. PROGRAM MONITORING AND CONTROL

Task 101   Testability Program Planning
Task 102   Testability Reviews
Task 103   Testability Data Collection and Analysis Planning

TASK SECTION 200. DESIGN AND ANALYSIS

Task 201   Testability Requirements
Task 202   Testability Preliminary Design and Analysis
Task 203   Testability Detail Design and Analysis

TASK SECTION 300. TEST AND EVALUATION

Task 301   Testability Inputs to Maintainability Demonstrations

5.2 Task integration. The individual task requirements provide for integration with other specified engineering and management tasks to preclude duplication and overlap while assuring timely consideration and accomplishment of testability requirements.

6. NOTES

6.1 Data requirements. When this standard is used in an acquisition, the data identified below shall be deliverable only when specified on the DD Form 1423 Contract

Data Requirement List (CDRL). When the DD Form 1423 is not used and Defense Acquisition Regulation 7-104.9(n) (2) is cited, the data identified below shall be delivered in accordance with requirements specified in the contract or purchase order. Deliverable data associated with the requirements of this standard are cited in the following tasks:

Task	Data Requirement	Applicable Data Item Description (DID)
101	Testability Program Plan	DI-T-7198
102	Program Review Documentation	DI-E-5423*
103	Data Collection and Analysis Plan	DI-R-7105
201, 202, 203	Testability Analysis Report	DI-T-7199
301	Maintainability Demonstration Test Plan	DI-R-7112
	Maintainability Demonstration	DI-R-7113

*Equivalent approved DID may be used.

(Copies of DIDs required by contractors in connection with specific acquisition functions should be obtained from the Naval Publications and Forms Center or as directed by the contracting officer.)

Custodians: Preparing Activity:
 Army CR   Navy-EC
 Navy EC
 Air Force 17   (Project ATTS-0007)

Review:

User:

TASK SECTION 100

PROGRAM MONITORING AND CONTROL

TASK 101
TESTABILITY PROGRAM PLANNING

101.1 **PURPOSE.** To plan for a testability program which will identify and integrate all testability design management tasks required to accomplish program requirements.

101.2 **TASK DESCRIPTION**

101.2.1 Identify a single organizational element within the performing activity which has overall responsibility and authority for implementation of the testability program. Establish analyses and data interfaces between the organizational element responsible for testability and other related elements.

101.2.2 Develop a process by which testability requirements are integrated with other design requirements and disseminated to design personnel and subcontractors. Establish controls for assuring that each subcontractor's testability practices are consistent with overall system or equipment requirements.

101.2.3 Identify testability design guides and testability analysis models and procedures to be imposed upon the design process. Plan for the review, verification and utilization of testability data submissions.

101.2.4 Develop a testability program plan which describes how the testability program will be conducted. The testability program plan shall be included as part of the systems engineering management plan or other integrated planning documents when required. The plan describes the time phasing of each testability task included in the contractual requirements and its relationship to other tasks.

101.3 **TASK INPUT**

101.3.1 Identification of each testability task which is required to be performed as part of the testability program.*

101.3.2 Identification of the time period over which each task is to be conducted.*

101.3.3 Identification of approval procedures for plan updates.*

101.3.4 Identification of deliverable data items.*

101.4 **TASK OUTPUT**

101.4.1 Testability program plan in accordance with DI-T-7198 if specified as a standalone plan. When required to be a part of another engineering or management plan, use appropriate, specified DID.

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*To be specified by the requiring authority.

TASK 102
TESTABILITY REVIEWS

102.1 PURPOSE. To establish a requirement for the performing activity to (1) provide for all official review of testability design information in a timely and controlled manner, and (2) conduct in-process testability design reviews at specified dates to ensure that the program is proceeding in accordance with the contract requirements and program plans.

102.2 TASK DESCRIPTION

102.2.1 Include the formal review and assessment of the testability program as an integral part of each system program review (e.g., system design review, preliminary design review, critical design review, etc.) specified by the contract. Reviews shall cover all pertinent aspects of the testability program such as:

    a.   Status and results of testability-related tasks.
    b.   Documentation of task results in the testability analysis report.
    c.   Testability-related requirements in specifications.
    d.   Testability design, cost or schedule problems.

102.2.2 Conduct and document testability design reviews with performing activity personnel and with subcontractors and suppliers. Coordinate and conduct testability reviews, in conjunction with reliability, maintainability and logistic support reviews whenever possible. Inform the requiring authority in advance of each review. Design reviews shall cover all pertinent aspects of the design such as the following:

    a.   Review the impact of the selected diagnostic concept on readiness, life cycle costs, manpower and training.

    b.   Review performance monitoring, built-in test and off-line test performance requirements and constraints to ensure that they are complete and consistent.

    c.   Review the rationale for the inherent testability criteria and weighting factors selected.

    d.   Review the testability techniques employed by the design groups. Identify testability design guides or procedures used. Describe any testability analysis procedures or automated tools to be used.

    e.   Review the extent to which testability criteria are being met. Identify any technical limitations or cost considerations inhibiting full implementation.

    f.   Review adequacy of Failure Modes and Effects Analysis (FMEA) data as a basis for test design. Assess adequacy of testability/FMEA data interface.

g.   Review coordination between BIT hardware and BIT software efforts. Review BIT interface to operator and maintenance personnel.

h.   Review BIT fault detection and fault isolation measures to be used. Identify models used and model assumptions. Identify any methods to be used for automatic test generation and test grading.

i.   Review BIT fault detection and fault isolation performance to determine if BIT specifications are met. Review efforts to improve BIT performance through improved tests or item redesign. Assess adequacy of testability/maintainability data interfaces.

j.   Review testability parameters to be included in Maintainability Demonstration. Identify procedures through which testability concerns are included in Demonstration Plans and Procedures.

k.   Review compatibility of signal characteristics at selected test points with planned test equipment. Assess adequacy of data interface between testability and Support and Test Equipment organizational elements.

l.   Review performance monitoring, BIT design and off-line test requirements to determine completeness and consistency.

m.   Review approaches to monitoring production testing and field maintenance actions to determine fault detection and fault isolation effectiveness.

n.   Review plans for evaluating impact on testability for Engineering Change Proposals.

102.3   TASK INPUT

102.3.1   Identification of amount of time to be devoted to the testability program at each formal review and the level of technical detail to be provided.*

102.3.2   Identification of level of participation desired by the requiring authority in internal and subcontractor testability design reviews.*

102.4   TASK OUTPUT

102.4.1   Documented results of testability assessment as an integral part of system program review documentation. (102.2.1)

102.4.2   Documented results of testability design reviews, including action items pending. (102.2.2)

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*To be specified by the requiring authority.

TASK 103
TESTABILITY DATA COLLECTION AND ANALYSIS PLANNING

103.1 **PURPOSE.** To establish a method for identifying and tracking testability-related problems during system production and deployment and identifying corrective actions.

103.2 TASK DESCRIPTION

103.2.1 Develop a plan for the analysis of production test results to determine if BIT hardware and software, ATE hardware and software, and maintenance documentation are meeting specifications in terms of fault detection, fault resolution, fault detection times and fault isolation times.

103.2.2 Develop a plan for the analysis of maintenance actions for the fielded system to determine if BIT hardware and software, ATE hardware and software, and maintenance documentation are meeting specifications in terms of fault detection, fault resolution, false indications, fault detection times and fault isolation times.

103.2.3 Define data collection requirements to meet the needs of the testability analysis. The data collected shall include a description of relevant operational anomalies and maintenance actions. Data collection shall be integrated with similar data collection procedures, such as those for reliability and maintainability, and Logistic Support Analysis and shall be compatible with specified data systems in use by the military user organization.

103.3 TASK INPUT

103.3.1 Identification of field or depot test equipment (either government furnished equipment or contractor furnished equipment) to be available for production and deployment testing.*

103.3.2 Identification of existing data collection systems in use by the using command.*

103.3.3 Relationship of Task 103 to Task 104 of MIL-STD-785 and Task 104 of MIL-STD-470.*

103.4 TASK OUTPUT

103.4.1 Testability data collection and analysis plan for production test; documented in accordance with DI-R-7105. (103.2.1)

103.4.2 Testability data collection and analysis plan for analyzing maintenance actions on fielded systems; documented in accordance with DI-R-7105. (103.2.2 and 103.2.3).

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*To be specified by the requiring authority.

TASK SECTION 200

DESIGN AND ANALYSIS

TASK 201
TESTABILITY REQUIREMENTS

201.1   PURPOSE. To (1) recommend system test and testability requirements which best achieve availability and supportability requirements and (2) allocate those requirements to subsystems and items.

201.2   TASK DESCRIPTION

201.2.1 Establish overall testability design objectives, goals, thresholds and constraints in support of the logistic support analysis process of MIL-STD-1388-1 or equivalent supportability analysis approved by the requiring authority. In this analysis, prime system design for testability is to be one of the elements to be traded off for improved supportability. Inputs to these requirements include:

      a.   Identification of technology advancements which can be exploited in system development and test development and which have the potential for increasing testing effectiveness, reducing test equipment requirements, reducing test costs, or enhancing system availability.

      b.   Identification of existing and planned test resources (e.g., family of testers in inventory) which have potential benefits. Identify tester limitations.

      c.   Identification of testing and testability problems on similar systems which should be avoided.

201.2.2 Establish performance monitoring, built-in test and off-line test objectives for the new system at the system and subsystem levels. Identify the risks and uncertainties involved in achieving the objectives established.

201.2.3 Establish BIT, test equipment and testability constraints for the new system, such as limitations on additional hardware for BIT, for inclusion in system specifications or other requirement documents. These constraints shall include both quantitative and qualitative constraints.

201.2.4 Evaluate alternative diagnostic concepts to include varying degrees of BIT, manual and off-line automatic testing, diagnostic test points, etc., and identify the selected diagnostic concept. The evaluation shall include:

      a.   A determination of the sensitivity of system readiness parameters to variations in key testability parameters. These parameters include BIT fault detection, false alarm rate, etc.

      b.   A determination of the sensitivity of life cycle costs to variations in key testability parameters.

      c.   An estimation of the manpower and personnel implications of alternative diagnostic concepts in terms of direct maintenance manhours per operating hour, job classifications, skill levels, and experience required at each level of maintenance.

d.   An estimation of risk associated with each concept.

201.2.5 Establish BIT performance requirements at the system and subsystem level. These requirements include specific numeric performance requirements imposed by the requiring authority. Other requirements shall be based, in part, on:

a.   Maximum allowable time between the occurrence of a failure condition and the detection of the failure for each mission function.

b.   Maximum allowable occurrence of system downtime due to erroneous failure indications (BIT false alarms).

c.   Maximum allowable system downtime due to corrective maintenance actions at the organizational level.

d.   Minimum life-cycle costs.

201.2.6 Recommend BIT and testability requirements for inclusion in system specifications. Appendix A, Figure 5, provides guidance on requirements to be specified.

201.2.7 Allocate BIT and testability requirements to configuration item specifications based upon reliability and criticality considerations.

201.3   TASK INPUT

201.3.1 Supportability analysis data in accordance with MIL-STD-1388-1 or other method approved by the requiring authority.

201.3.2 Reliability and maintainability analysis and requirements such as from Task 203 of MIL-STD-785 and Task 205 of MIL-STD-470.

201.3.3 Specific numeric BIT and testability requirements.*

201.4   TASK OUTPUT

201.4.1 Testability data required for supportability analysis.   (201.2.1 through 201.2.4)

201.4.2 Description of selected diagnostic concept and tradeoff methodology, evaluation criteria, models used, and analysis results; documented in accordance with DI-T-7199.   (201.2.4)

201.4.3 Recommended BIT and testability requirements for system specification. (201.2.3, 201.2.5 and 201.2.6)

201.4.4 Recommended BIT and testability requirements for each configuration item specification. (201.2.7)

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*To be specified by the requiring authority.

TASK 202
TESTABILITY PRELIMINARY DESIGN AND ANALYSIS

202.1 PURPOSE. To incorporate testability design practices into the design of a system or equipment early in the design phase and to assess the extent to which testability is incorporated.

202.2 TASK DESCRIPTION

202.2.1 Institute testabilty design concepts as an integral part of the system or equipment design process. Guidance is provided in Appendix A, paragraph 50.6, on the use of these concepts.

202.2.2 Incorporate appropriate testability design concepts into the preliminary design for each item. Develop BIT hardware, software and firmware as an integral part of the design effort.

202.2.3 Analyze and evaluate the selected testability concepts of the system or equipment design in a qualitative manner to ensure that the design will support the required level of testing. Conduct an analysis of the inherent (intrinsic) testability of the preliminary design. The analysis identifies the presence or absence of hardware features which facilitate testing and identifies problem areas. The method of Appendix B shall be applied to each item identified for inherent testability assessment by the requiring authority. The inputs required by Appendix B shall be determined by the performing activity and approved by the requiring authority.

202.2.4 Modify the design, as necessary, until the inherent testability equals or exceeds the threshold value. If the performing activity concludes that achieving the threshold is not possible or cost effective, but that the fault detection and fault isolation requirements will be met, the performing activity shall provide supporting data for review by the requiring authority.

202.2.5 Develop a methodology for Task 203 for predicting fault detection and fault isolation performance levels.

202.3 TASK INPUT

202.3.1 System or equipment design data.

202.3.2 Identification of items to be included in inherent testability analysis (Appendix B).*

202.3.3 For each item, inherent testability threshold value to be achieved.* Guidance for establishing a threshold value is given in Appendix A, paragraph 50.6.11.3.

202.4 TASK OUTPUT

202.4.1 System or equipment design which incorporates testability features. (202.2.1, 202.2.2 and 202.2.4)

202.4.2 Description of testability design tradeoffs and testability features selected for implementation; documented in accordance with DI-T-7199. (202.2.2 and 202.2.4)

202.4.3 For each item, assignment of weighting factor and scoring method for each testability criterion (Appendix B). (202.2.3)

202.4.4 Inherent testability assessment; documented in accordance with DI-T-7199. (202.2.3)

202.4.5 Description of methodologies, models and tools to be used in Task 203; documented in accordance with DI-T-7199. (202.2.5)

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*To be specified by the requiring authority.

TASK 203
TESTABILITY DETAIL DESIGN AND ANALYSIS

203.1   PURPOSE. To incorporate features into the design of a system or equipment which will satisfy testability performance requirements and to predict the level of test effectiveness which will be achieved for the system or equipment.

203.2   TASK DESCRIPTION

203.2.1 Incorporate testability design features, including BIT, into the detailed design for each item.

203.2.2 Analyze that all critical functions of the prime equipment are exercised by testing to the extent specified. The performing activity shall conduct functional test analysis for each configuration item (CI) and for each physical partition of the CI designated as a UUT.

203.2.3 Conduct an analysis of the test effectiveness of BIT and off-line test.

      a.   Identify the failures of each component and the failures between components which correspond to the specified failure modes for each item to be tested. These failures represent the predicted failure population and are the basis for test derivation (BIT and off-line test) and test effectiveness evaluation. Maximum use shall be made of a failure modes and effects analysis (FMEA), from Task 204 of MIL-STD-470A, if a FMEA is required. The FMEA requirements may have to be modified or supplemented to provide the level of detail needed.

      b.   Model components and interconnections for each item such that the predicted failure population may be accurately modeled. The performing activity shall develop or select models which are optimum considering accuracy required, cost of test generation and simulation, standardization and commonality.

      c.   Analyze and evaluate the effectiveness of planned testing based upon the predicted failure population. The analysis shall give particular emphasis to fault detection and fault isolation for critical and high failure rate items and interconnections. The test effectiveness data shall be used to guide redesign of equipment and test programs, as required, and to assist in the prediction of spares requirements.

      d.   Prepare justification for any classes of faults which are undetected, cannot be isolated or are poorly isolated when using the developed test stimuli and submit to the requiring authority for review. Prepare additional or alternate diagnostic approaches. Identify hard to test faults to the LSA process.

203.2.4 Iterate the design of the prime item built-in test until each predicted test effectiveness value equals or exceeds the specified value.

203.2.5 Develop system-level BIT hardware and software, integrating the built-in test capabilities of each subsystem/item.

203.2.6 Predict the level of BIT fault detection for the overall system based upon the BIT detection predictions, weighted by failure rate, of the individual items, including

GFE. Predict the level of fault isolation for the overall system through system-level test. Predict the probability of BIT false alarms for the overall system.

203.2.7 Assemble cost data associated with BIT and design for testability on a per unit basis (e.g., additional hardware, increased modularity, additional connector pins, etc.). Extract and summarize cost data associated with the implementation of the testability program, test generation efforts and production test. Provide test effectiveness predictions as inputs to availability and life cycle cost analyses.

203.2.8 Incorporate BIT and testability corrective design actions as determined by the maintainability demonstration results and initial testing.

203.2.9 Incorporate changes and corrections into testability models, test generation software, etc., which reflect an improved understanding of operations and failure modes as the design progresses. Use updated models, software, etc., to update test effectiveness predictions as necessary.

203.3   TASK INPUT

203.3.1 Identification of items to be included in test effectiveness predictions.*

203.3.2 System or item preliminary design data. '

203.3.3 BIT specification.

203.3.4 Identification of failure modes and effects and failure rates for each item from Task 204 of MIL-STD-470A.

203.3.5 Test effectiveness data for GFE.*

203.3.6 Corrective action recommendations from maintainability demonstration.

203.4   TASK OUTPUT

203.4.1 System or item design which meets testabilty and maintainability requirements. (203.2.1, 203.2.4, 203.2.5 and 203.2.8)

203.4.2 Description of built-in test and testability features for each item designated as a Unit Under Test; documented in appropriate Test Requirements Document. (203.2.1)

203.4.3 Test effectiveness prediction for each item; data provided in support of Task 205 of MIL-STD-470A and Task 401 of MIL-STD-1388-1A and documented in accordance with DI-T-7199. (203.2.2, 203.2.3, 203.2.7 and 203.2.9)

203.4.4 System test effectiveness prediction; data provided in support of Task 205 of MIL-STD-470A and documented in accordance with DI-T-7199. (203.2.6, 203.2.7 and 203.2.9)

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*To be specified by the requiring authority.

TASK SECTION 300

TEST AND EVALUATION

TASK 301
TESTABILITY INPUTS TO MAINTAINABILITY DEMONSTRATION

301.1   PURPOSE. To determine compliance with specified testability requirements and assess the validity of testability predictions.

301.2   TASK DESCRIPTIONS

301.2.1 Determine how testability requirements are to be demonstrated using maintainability demonstration, test program verification or other demonstration methods. The following elements are to be demonstrated to the extent each is specified in the contractual documents:

    a.   The ability of operational system checks to detect the presence of errors.

    b.   The ability of system or subsystem BIT to detect and isolate failures.

    c.   The compatibility of each item as a UUT with the selected test equipment.

    d.   The ability of the test equipment and associated TPSs to detect and isolate failures.

    e.   The adequacy of technical documentation with respect to fault dictionaries, probing procedures, manual troubleshooting, theory of operation, etc.

    f.   The correlation of BIT fault detection and fault isolation indications with off-line test results.

    g.   The validity of models used to predict testability parameters.

301.2.2 Develop plans for the demonstration of testability parameters and integrate into the plans and procedures for maintainability demonstration.

301.2.3 Conduct additional demonstrations, as needed, using the methods and criteria of MIL-STD-471 and MIL-STD-2077 as appropriate, to obtain sufficient testability data for evaluation and document as a portion of the testability demonstration results. The demonstrations are to be combined with other demonstrations whenever practical.

301.3   TASK INPUT

301.3.1 Identification of items to be demonstrated.*

301.3.2 Identification of MIL-STD-471 test method or alternative procedure for conducting a maintainability demonstration.*

301.3.3 Identification of MIL-STD-2077 quality assurance procedure or alternative procedure for evaluation of TPSs.*

301.4 <u>TASK OUTPUT</u>

301.4.1 Testability demonstration plan; documented in accordance with DI-R-7112.
(301.2.2)

301.4.2 Testability demonstration results; documented in accordance with DI-R-7113.
(301.2.3)

*To be specified by the requiring authority.

APPENDIX A
TESTABILITY PROGRAM APPLICATION GUIDANCE

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CONTENTS (Continued)

APPENDIX A

CONTENTS (Continued)

ILLUSTRATIONS

TABLES

APPENDIX A
TESTABILITY PROGRAM APPLICATION GUIDANCE

10. SCOPE

10.1 **Purpose**. This appendix provides rationale and guidance for the selection and tailoring of tasks to define a testability program which meets established program objectives. No contractual requirements are contained in this Appendix.

20. REFERENCED DOCUMENTS

20.1 **Issues of Documents**. The following documents form a part of this Appendix for guidance purposes.

STANDARDS

    MILITARY

MIL-STD-781	Reliability Design Qualification and Product Acceptance Tests: Exponential Distribution
MIL-STD-1345 (Navy)	Test Requirements Documents, Preparation of
MIL-STD-1519 (USAF)	Test Requirements Documents, Preparation of
MIL-STD-2076	UUT Compatibility with ATE, General Requirements for

PUBLICATIONS

    JOINT SERVICE

NAVMATP 9405 DARCOM 34-1 AFLCP 800-39 AFSCP 800-39 NAVMC 2721 19 March 1981	Joint Service Built-in Test Design Guide
Naval Fleet Analysis Center TM 824-1628 1 October 1983	Joint Service Electronic Design for Testability Course Notes

    TECHNICAL REPORTS

Naval Air Systems Command 1 August 1979 Contract N000140-79-C-0896	Avionic Design Guide for ATE Compatibility

Air Force Aeronautical Systems Division September 1983 Contract F33657-78-C-0502	Modular Automatic Test Equipment Guide 3-Avionics Testability Design Guide
Air Force Rome Air Development Center December 1979 RADC-TR-79-309	BIT/External Test Figures of Merit and Demonstration Techniques
Naval Fleet Analysis Center 2 November 1984 TM-8243-1685	Testability Requirements Analysis Handbook

DIRECTIVE

DEPARTMENT OF DEFENSE

| DOD Directive 5000.39 | Acquisition and Management of Integrated Logistic Support for Systems and Equipment |

30. DEFINITIONS

30.1   Definitions.   The definitions included in MIL-STD-1309, MIL-STD-721 and Appendix C shall apply.

40. GENERAL APPLICATION GUIDANCE

40.1   Task selection criteria.   The selection of tasks which can materially aid the attainment of testability requirements is a difficult problem for both government and industry organizations faced with severe funding and schedule constraints.   This Appendix provides guidance for the selection of tasks based upon identified program needs.   Once appropriate testability program tasks have been selected, each task must be tailored in terms of timing, comprehensiveness and end products to meet the overall program requirements.

40.2   Testability program in perspective.   The planned testability program must be an integral part of the systems engineering process and serve as an important link between design and logistic support in accordance with DOD Directive 5000.39.   The tasks which influence and are influenced by the testability program are extracted from DOD Directive 5000.39 in the following paragraphs.

    a.   Concept exploration phase

        1.   Identify manpower, logistic, reliability, maintainability and testability parameters critical to system readiness and support costs.

        2.   Estimate what is achievable for each parameter.

b.   Demonstration and validation (D&V) phase

1.   Conduct tradeoffs among system design characteristics and support concepts.

2.   Establish consistent set of goals and thresholds for readiness, reliability, maintainability, BIT, manpower and logistic parameters.

3.   Establish test and evaluation (T&E) plans to assess achievement of support-related thresholds.

c.   Full scale development (FSD) phase

1.   Perform detailed analysis and tradeoffs of design, reliability and maintainability (R&M), manning levels and other logistic requirements.

2.   Perform T&E of adequacy of planned manpower, support concepts, R&M and testability to meet system readiness and utilization objectives.

d.   Production and deployment phase

1.   Perform follow-on evaluation of maintenance plan, support capability, operation and support costs and manpower.

2.   Correct deficiencies.

40.3   System testability program (Figure 1). For major systems, the testability tasks for each program phase are summarized in Table I and listed below.

a.   Concept exploration phase - Establish testability objectives in preliminary system specification (Task 201).

b.   D&V phase

1.   Prepare testability program plan (Task 101).

2.   Incorporate testability features into D&V items and evaluate effectiveness (See 40.4).

3.   Select alternative system concept(s). Establish testability requirements in system specification. Allocate testability requirements to item development specifications (Task 201).

4.   Conduct testability review as part of system design review (Task 102).

c.   FSD phase

1.   Prepare and revise testability program plan (Task 101).

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Figure 1. System Testability Program Flow Diagram (Sheet 1 of 3)

FSD PHASE

D&V PHASE

(CONTINUED FROM FIGURE 1, SHEET 1)

SYSTEM SPECIFICATION TESTABILITY REQUIREMENTS

ITEM SPECIFICATION TESTABILITY REQUIREMENTS

101.2.1 PREPARE TESTABILITY PROGRAM PLAN

202.2.1 IMPOSE TESTABILITY DESIGN DISCIPLINE

PERFORM TESTABILITY DESIGN AND EVALUATION OF EACH ITEM (SEE FIGURE 2)

203.2.5 DEVELOP SYSTEM-LEVEL BIT HARDWARE, SOFTWARE, AND FIRMWARE

(REFER TO FIGURE 1, SHEET 3)
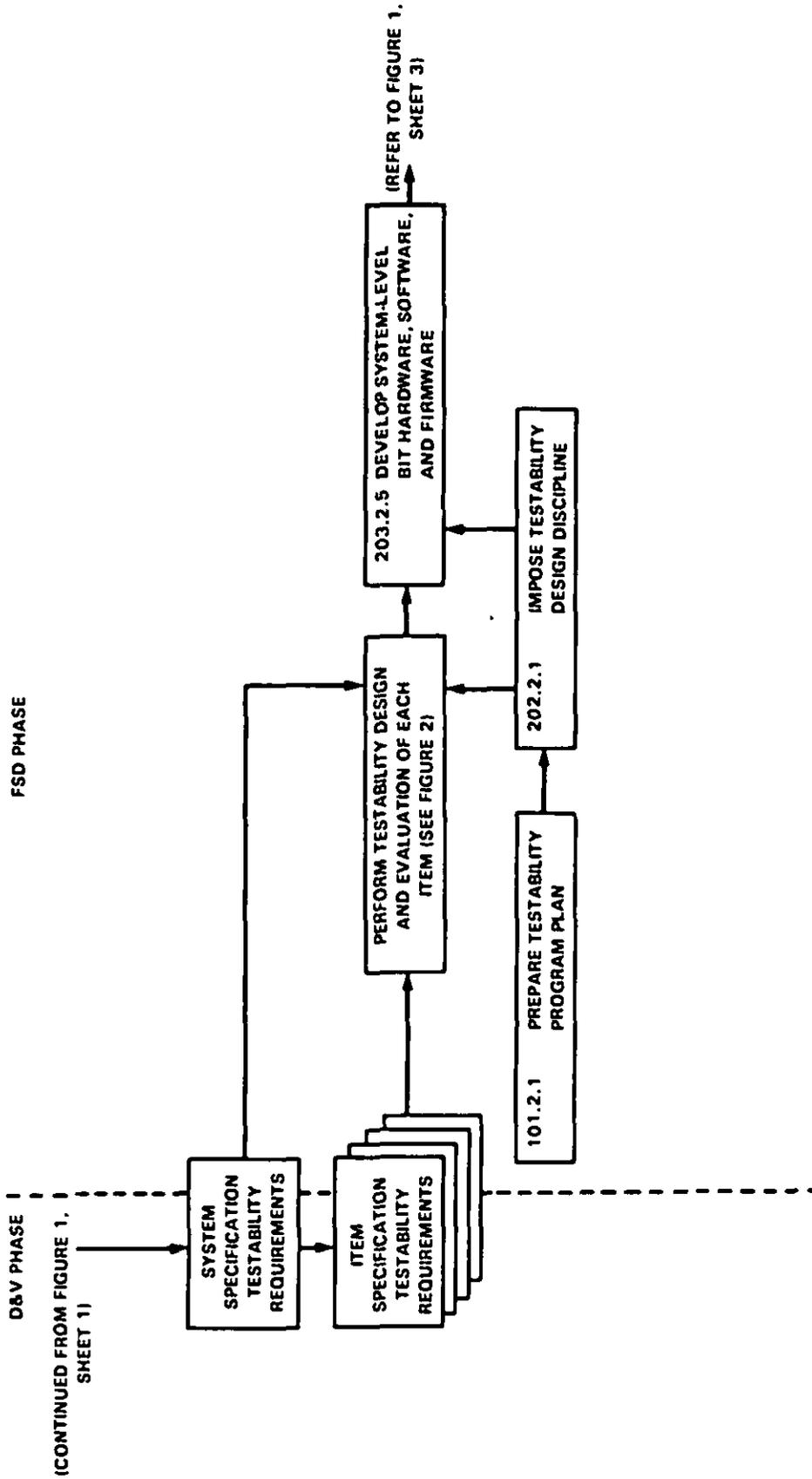
Figure 1. System Testability Program Flow Diagram (Sheet 2 of 3)
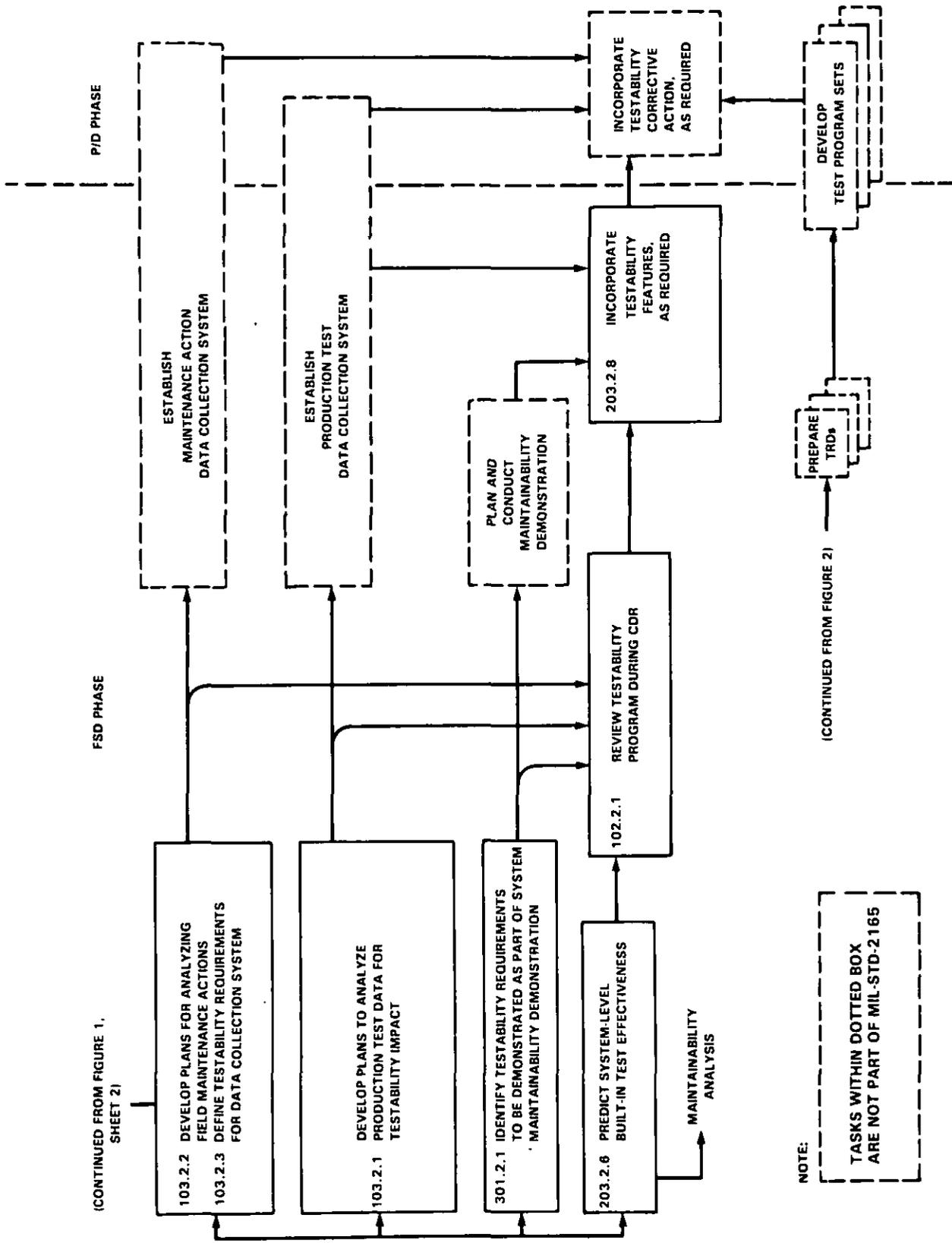
Figure 1. System Testability Program Flow Diagram (Sheet 3 of 3)

Table L Task application guidance matrix.

Task		CON	Program Phase D&V	FSD	P/D
101	Testability program planning	NA	G	G	NA
102	Testability reviews	G[1]	G	G	S
103	Testability data collection and analysis planning	NA	S	G	G
201	Testability requirements	G[1]	G	G	NA
202	Testability preliminary design and analysis	NA	S	G	S
203	Testability detail design and analysis	NA	S	G	S
301	Testability demonstration	NA	S	G	S

NA - Not applicable
G - Generally applicable
S - Selectively applicable to high risk items during D&V, or to design changes during P&D

CON - Concept Exploration
D&V - Demonstration and Validation
FSD - Full Scale Development
P/D - Production/Deployment

NOTES:

[1] MIL-STD-1388 is primary implementation document for diagnostic requirements tradeoffs and review as part of logistics support analysis during Concept Exploration phase.

   2.   Incorporate testability features into FSD items and evaluate effectiveness (See 40.4).

   3.   Demonstrate system testability effectiveness (Task 301).

   d.   Production and deployment phase – Collect data on achieved testability effectiveness. Take corrective action, as is necessary.

40.4   Item testability program (Figure 2). For all items, whether developed as a subsystem under a system acquisition program or developed under an equipment acquisition program, the testability tasks are listed below.

   a.   Preliminary design

   1.   Prepare testability program plan, if a plan was not developed as part of a system acquisition program (Task 101).

   2.   Incorporate testability features into preliminary design (Task 202).

   3.   Prepare inherent testability checklist for each item (Task 202).

   4.   Conduct testability review as part of preliminary design review (Task 102).

   b.   Detail design

   1.   Incorporate testability features into detail design (Task 203), and predict inherent testability for each item (Task 202).

   2.   Predict test effectiveness for each item (Task 203).

   3.   Conduct testability review as part of the critical design review (Task 102).

   4.   Demonstrate item testability effectiveness (Task 301).

40.5   Criteria for imposing a testability program during the D&V phase. During the D&V phase, a formal testability program should be applied to the system integration effort and, in addition, should be selectively applied to those subsystems which present a high risk in testing. The high risk aspect of test design may be a result of:

   a.   Criticality of function to be tested,

   b.   Difficulty of achieving desired test quality at an affordable cost,

   c.   Difficulty of defining appropriate testability measures or demonstrations for technology being tested,
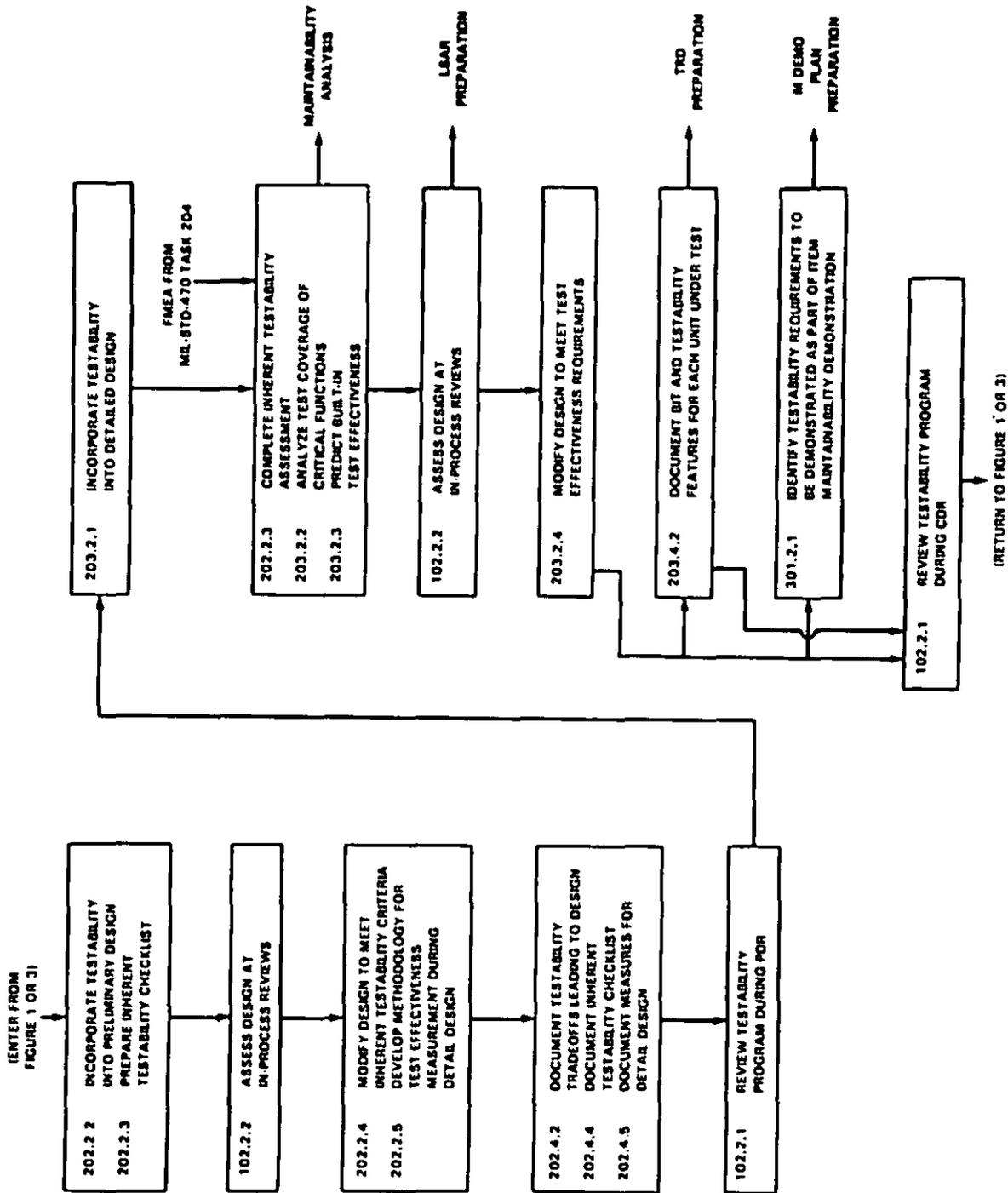
Figure 2. Item Testability Design Detailed Flow Diagram

     d.   Large impact on maintainability or elements if expected test quality, automation, throughput, etc., is not achieved, or

     e.   High probability that modifications to the subsystem during FSD will be limited.

40.6   **Equipment testability program (Figure 3).**   For the acquisition of less-than-major systems or individual equipments, the testability tasks are listed below.

     a.   Establish system or equipment testability requirements (performed by requiring authority using Task 201 as guidance).

     b.   Prepare testability program plan (Task 101).

     c.   Incorporate testability features into items and evaluate effectiveness (See 40.4).

     d.   Collect data on achieved testability effectiveness (performed by requiring authority using Task 103 as guidance).

40.7   **Iterations.**   Certain tasks contained in this standard are highly iterative in nature and recur at various times during the acquisition cycle, proceeding to lower levels of hardware indenture and greater detail in the classical systems engineering manner.

50. DETAILED APPLICATION GUIDANCE

50.1   Task 101 – Testability program planning

50.1.1   Scope.   The testability program plan is the basic tool for establishing and executing an effective testability program.   The testability program plan should document what testability tasks are to be accomplished, how each task will be accomplished, when they will be accomplished, and how the results of the task will be used.   The testability program plan may be a stand-alone document but preferably should be included as part of the systems engineering planning when required.   Plans assist the requiring authority in evaluating the prospective performing activities approach to and understanding of the testability task requirements, and the organizational structure for performing testability tasks.   The testability program plan should be closely coordinated with the maintainabiliaty program plan.

50.1.2   Submission of plan.   When requiring a testability program plan, the requiring authority should allow the performing activity to propose specifically tailored tasks with supporting rationale to show overall program benefits.   The testability program plan should be a dynamic document that reflects current program status and planned actions. Accordingly, procedures must be established for updates and approval of updates by the requiring authority when conditions warrant.   Program schedule changes, test results, or testability task results may dictate a change in the testability program plan in order for it to be used effectively as a management document.
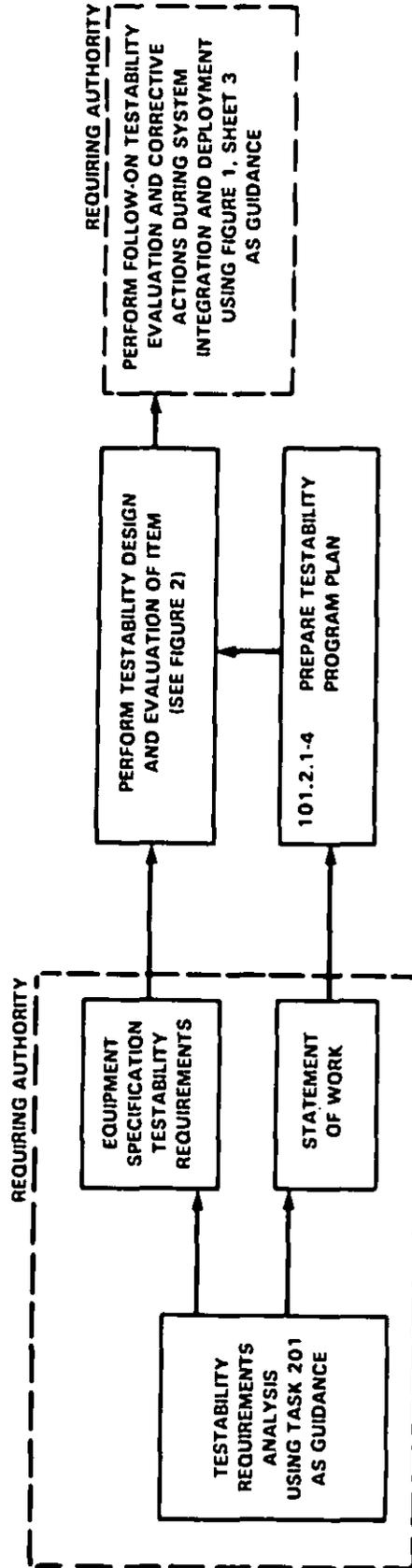
Figure 3. Equipment Testability Program Flow Diagram

50.1.3 Plan for D&V phase. When submitted at the beginning of a D&V phase, the testability program plan should highlight the methodology to be used in establishing qualitative and quantitative testability requirements for the system specification. The plan should also describe the methodology to be used in allocating quantitative system testability requirements down to the subsystem or configuration item level. The nature of the D&V phase will vary considerably from program to program, ranging from a "firming up" of preliminary requirements to a multi-contractor "fly off" of competing alternatives. In all cases, sufficient data must be furnished to the Government to permit a meaningful evaluation of testing and testability alternatives. The testability program plan should indicate how the flow of information is to be accomplished: through informal customer reviews, through CDRL·data submissions, and through testability reviews as an integral part of SDR.

50.1.4 Organizational interfaces. In order to establish and maintain an effective testability program, the testability manager must form a close liaison with all design disciplines. In satisfying system support requirements, the prime system design must be treated as one of the elements which may be traded off through the supportability analysis process. As a result, the testability manager must be prepared to work aggressively with design engineers to ensure a proper balance between performance, cost and supportability. It is not efficient or effective for the testability manager to assume the role of post-design critic and risk large cost and schedule impacts. The testability influence must be apparent from the initiation of the design effort, through design guidelines, training programs, objective measures, etc.

50.2 Testability analysis report

50.2.1 Content. The testability analysis report collects a number of different testability task results and documents the results in a single, standard format. The testability analysis report should be updated at least prior to every major program review and this requirement must be reflected in the CDRL. The actual content and level of detail in each submission of the testability analysis report will depend upon the program phase. Table II provides guidance as to which tasks/subtasks would be included for review by the requiring authority prior to four specific reviews. The first entry for a subtask indicates the time of initial submission. Any following entries indicate one or more updates to the original data as the design becomes defined in greater detail.

50.2.2 Utilization. The testability analysis report should be used by the performing activity to disseminate all aspects of the testability design status to the various organizational elements. As such, the testability analysis report should be considered to be a dynamic document, containing the latest available design information and issued under an appropriate degree of configuration control. As a minimum, the testability analysis report should accurately reflect the latest design data when informal testability design reviews are held.

50.2.3 TRD interface. The testability analysis performed during the FSD phase and documented in the testability analysis report should be used as a partial basis for the TRD for each UUT. The TRD, developed in accordance with MIL-STD-1519 or MIL-STD-1345, constitutes the formal interface between the activity responsible for detailed

Table II. Testability Analysis Report application guidance matrix

Subtask Output		SDR	PDR	CDR	FQR
201.4.2	Requirements tradeoffs	X	X		
202.4.2	Design tradeoffs	X	X	X	
202.4.2	Testability design data		X	X	
202.4.3	Inherent testability checklist		X		
202.4.4	Inherent testability assessment		X	X	
202.4.5	Detail design analysis procedures		X	X	
203.4.3	Item test effectiveness prediction			X	X
203.4.4	System test effectiveness prediction			X	X

Note: Each submission of the Testability Analysis Report should be required by the CDRL to be delivered sufficiently in advance of each review such that the requiring authority may review the material.

hardware design and the activity responsible for TPS development. This document serves as a *single source of all performance verification and diagnostic procedures, and for all* equipment requirements to support each UUT in its maintenance environment, whether supported manually or by ATE. The TRD also provides detailed configuration identification *for UUT design and test requirements data to ensure compatible test* programs.

50.2.4 Classified data. If classified data is required to document the testability analysis, it should be placed in a separate attachment to the testability analysis report such that the testability analysis report may have the widest possible distribution.

50.3 Task 102 – Testability review

50.3.1 Type of review. This task is directed toward two types of review: (1) formal system program reviews (Subtask 102.2.1), and (2) review of design information within the performing activity from a testability standpoint (Subtask 102.2.2). The second type provides testability specialists the authority with which to manage design tradeoffs. For most developers this type of review is a normal operating practice. Procedures for this type of review would be included in the testability program plan.

50.3.1.1 Program reviews. System program reviews such as preliminary design reviews and critical design reviews are an important management and technical tool of the requiring authority. They should be specified in statements of work to ensure adequate staffing and funding and are typically held periodically during an acquisition program to evaluate overall program progress, consistency, and technical adequacy. An overall testability program status should be an integral part of these reviews whether conducted with subcontractors or with the requiring authority.

50.3.1.2 Testabilty design reviews. Testability design reviews are necessary to assess the progress of the testability design in greater technical detail and at a greater frequency than is provided by system program reviews. The reviews shall ensure that the various organizational elements within the performing activity which impact or are impacted by testability are represented and have an appropriate degree of authority in making decisions. The results of performing activity's internal and subcontractor system reviews should be documented and made available to the requiring authority on request. These reviews should be coordinated, whenever possible, with maintainability, ILSMT and program management reviews.

50.3.2 Additional data review. In addition to formal reviews, useful information can often be gained from performing activity data which is not submitted formally, but which can be made available through an accession list. A data item for this list must be included in the CDRL. This list is a compilation of documents and data which the requiring authority can order, or which can be reviewed at the performing activity's facility.

50.4 Task 103 – Testability data collection and analysis planning

50.4.1 Testability effectiveness tracking. A testability program cannot be totally effective unless provisions are made for the systematic tracking and evaluation of testability effectiveness beyond the system development phase. The objective of this

task is to plan for the evaluation of the impact of actual operational and maintenance environments on the ability of production equipment to be tested. The effectiveness of testability design techniques for intermediate or depot level maintenance tasks is monitored and analyzed as part of this evaluation. Much of the actual collection and analysis of data and resulting corrective actions may occur beyond the end of the contract under which the testability program is imposed and may be accomplished by personnel other than those of the performing activity. Still, it is essential that the planning for this task be initiated in the FSD phase, preferably by the critical design review.

50.4.2   Data collection and analysis plans. Separate plans should be prepared for testability data collection and analysis during (1) production phase (Subtask 103.2.1) and (2) deployment phase (Subtask 103.2.2). The plans should clearly delineate which analysis data are to be reported in various documents, such as T&E reports, production test reports, factory acceptance test reports, etc.

50.4.3   Test maturation. Most test implementations, no matter how well conceived, require a period of time for identification of problems and corrective action to reach specified performance levels. This "maturing" process applies equally to BIT and off-line test. This is especially true in setting test tolerances for BIT and off-line test used to test analog parameters. The setting of test tolerances to achieve an optimum balance between failure detection and false alarms usually requires the logging of considerable test time. It should be emphasized, however, that the necessity for "fine-tuning" a test system during production and deployment in no way diminishes the requirement to provide a "best possible" design during FSD. One way of accelerating the test maturation process is to utilize planned field or depot testers for portions of acceptance test. BIT test hardware and software should be exercised for those failures discovered and the BIT effectiveness documented and assessed.

50.4.4   Operational test and evaluation. The suitability of BIT should be assessed as an integral part of operational test and evaluation. A closed-loop data tracking system should be implemented to track initial failure occurrences, organizational-level corrective actions, subsequent higher-level maintenance actions, and subsequent utilization and performance of repaired and returned items. The data collection must be integrated as much as possible with similar data collection requirements such as those for tracking reliability and maintainability. The data tracking system must collect sufficient data to support the analysis of 50.4.4.1 through 50.4.4.3. All maintenance actions are first reviewed to determine if the failed item is relevant to BIT or off-line test. For example, items with loose bolts are not relevant to testability analysis. If at some point in the data tracking, an actual failure is found, the analysis for confirmed failures (50.4.4.1 and 50.4.4.2) is applied. If an actual failure is not found, the analysis for non-confirmed failures (50.4.4.3) is applied.

50.4.4.1 Confirmed failure, BIT.   For each confirmed failure, data on BIT effectiveness are analyzed:

    a.   Did BIT detect the failure?

    b.   Did BIT correctly indicate operational status to the operator?

c. Did BIT provide effective fault isolation information for corrective maintenance actions?

d. What was the ambiguity size (number of modules to be removed or further tested) due to fault localization or isolation by BIT?

e. How much time was required for fault isolation at the organizational level of maintenance?

50.4.4.2 _Confirmed failure, off-line test._ For each confirmed failure, data on off-line test compatibility are analyzed:

a. Were any workarounds required to overcome mechanical or electrical deficiencies in the UUT and ATE interface?

b. Did the ATE system provide failure detection results consistent with those of the initial detection by BIT?

c. Did the UUT design inhibit the ATE system from providing accurate fault isolation data?

50.4.4.3 Unconfirmed failure, BIT. For each unconfirmed failure situation (cannot duplicate) resulting from a BIT indication or alarm, the following data are analyzed:

a. What is the nature of the alarm?

b. What is the frequency of occurrence of the alarm?

c. What failure or failures are expected to cause the observed alarm?

d. What are the potential consequences of ignoring the alarm (in terms of crew safety, launching unreliable weapons, etc.)?

e. What are the operational costs of responding to the false alarm (in terms of aborted missions, degraded mode operation, system downtime)?

f. What are the maintenance costs associated with the false alarm?

g. What additional data are available from operational software dumps (e.g., soft failure occurrences) to characterize cannot duplicate occurrences?

50.4.5 Corrective action. The data on BIT effectiveness and off-line test compatibility are summarized and corrective action, if needed, is proposed by the performing activity or user activity. Those corrective actions dealing with redesign of the prime system are submitted for review and implementation as part of the established engineering change process.

50.5 Task 201 - Testability requirements

50.5.1 Supportability analysis interface. It is essential to conduct a Logistic Support Analysis or other supportability analyses (Subtask 201.2.1) early in an acquisition program to identify constraints, thresholds, and targets for improvement, and to provide supportability input into early system tradeoffs. It is during the early phases of an acquisition program that the greatest opportunity exists to influence the system design from a supportability standpoint. These analyses can identify supportability and maintainability parameters for the new system which are reasonably attainable, along with the prime drivers of support, manpower, personnel and training, cost, and readiness. The drivers, once identified, provide a basis for concentrated analysis effort to identify targets and methods of improvement. Mission and support systems definition tasks are generally conducted at system and subsystem levels early in the system acquisition process (Concept and D&V phases). Identification and analysis of risks plays a key role due to the high level of uncertainty and unknowns early in a system's life cycle. Performance of these tasks requires examination of current operational systems and their characteristics as well as projected systems and capabilities that will be available in the time frame that the new system will reach its operational environment. New system supportability and supportability related design constraints must be established based upon support systems and resources that will be available when the new system is fielded. Additional guidance may be found in the Testability Requirements Analysis Handbook (20.1).

50.5.2 New technology. Subtask 201.2.1a identifies new system supportability enhancements over existing systems through the application of new technology. This analysis will specify where improvements can be realized. It will identify the expected effect of improvements on supportability, cost and readiness values so that test equipment and testability objectives can be established. This task should be performed by design personnel in conjunction with supportability specialists.

50.5.3 Standardization. In many cases, utilization of existing support resources and personnel skills (Subtask 201.2.1b) can substantially reduce a system's life cycle cost, enhance the system's readiness, minimize the impact of introduction of the new system, and increase the mobility of the operational unit using the new system. Test system standardization requirements for new systems can also arise from Department of Defense or service support policies. Examples of these requirements can include standard software language requirements or use of standard multi-system test equipment.

50.5.4 Test objectives. The type of parameter (e.g., objectives, goals, thresholds) developed as a result of performing Task 201 will depend on the phase of development. Generally, during the Concept Exploration phase testing objectives will be established (Subtask 201.2.2). These objectives are established based on the results of previous mission and support systems definition tasks, especially the opportunities identified as a result of new technology, and are subject to tradeoffs to achieve the most cost effective solution to the mission need.

50.5.5 Diagnostic concept. The development of the diagnostic concept begins in the Concept Exploration phase and is refined as more detailed data becomes available during the D&V phase. Quantitative testability requirements would not normally be specified

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during the concept exploration phase. However, a preliminary estimate of the critical testability parameters should be made to ascertain if the required system availability and maintenance and logistic support concepts can be supported using testability parameters demonstrated as achievable on similar systems. The diagnostic concept usually evolves as follows:

      a. Determine on-line BIT requirements to ensure monitoring of critical functions and monitoring of functions which affect personnel safety.

      b. Determine additional on-line BIT requirements to support high system availability through redundant equipments and functions, backup or degraded modes of operation, etc.

      c. Determine additional BIT requirements to support confidence checks prior to system initiation or at periodic intervals during system operation.

As more detailed design data becomes available, usually during the D&V phase, the diagnostic concept further evolves, making extensive use of readiness and life cycle cost models:

      d. Determine what fault isolation capability is inherent in (a) through (c); determine additional BIT requirements to support the preliminary maintenance concept.

      e. Determine automatic, semi-automatic and manual off-line test requirements to fill voids due to technical or cost limitations associated with using BIT.

Note: The sum of the requirements for BIT, off-line automatic test, semi-automatic test and manual test must always provide for a complete (100%) maintenance capability at each maintenance level.

      f. Determine what existing organizational level BIT capabilities are usable at the next higher maintenance level. Determine requirements for ATE, general purpose electronic test equipment (GPETE) and technical documentation to provide, with BIT, the total maintenance capability.

If testability requirements are included in a preliminary system specification, they should be qualitative in nature pending the more quantitative tradeoffs of the D&V design. Figure 4 provides some model paragraphs which may be included primarily to alert the performing activity that design for testability is considered to be an important aspect of design and that quantitative requirements will be imposed in the final system specification. Alternatively, the model paragraphs for the system specification, figure 5, could be used in the preliminary system specification with all quantitative requirements "to be determined."

    50.5.6 <u>Testability requirements.</u> Prior to the Full Scale Development phase, firm testability requirements are established (Subtasks 201.2.5) which are not subject to tradeoff. These represent the minimum - essential levels of performance that must be satisfied. Overall system objectives, goals and thresholds must be allocated and translated to arrive at testability requirements to be included in the system specification

3.X.X   Design for testability

3.X.X.1   Partitioning. The system shall be partitioned based, in part, upon the ability to confidently isolate faults.

3.X.X.2   Test points. Each item within the system shall have sufficient test points for the measurement or stimulus of internal circuit nodes so as to achieve an inherently high level of fault detection and isolation.

3.X.X.3   Maintenance capability. For each level of maintenance, BIT, off-line automatic test and manual test capabilities shall be integrated to provide a consistent and complete maintenance capability. The degree of test automation shall be consistent with the proposed personnel skill levels and corrective and preventive maintenance requirements.

3.X.X.4   BIT. Mission critical functions shall be monitored by BIT. BIT tolerances shall be set to optimize fault detection and false alarm characteristics. BIT indicators shall be designed for maximum utilization by intended personnel (operator or maintainer).

Figure 4. Model paragraphs, preliminary system specification.

3.X.X   Design for testability

a.   Requirement for status monitoring.

b.   Definition of failure modes, including interconnection failures, specified to be the basis for test design.

c.   Requirement for failure coverage (% detection) using full test resources.

d.   Requirement for failure coverage using BIT.

e.   Requirement for failure coverage using only the monitoring of operational signals by BIT.

f.   Requirement for maximum failure latency for BIT.

g.   Requirement for maximum acceptable BIT false alarm rate; definition of false alarm.

h.   Requirement for fault isolation to a replaceable item using BIT.

i.   Requirement for fault isolation times.

j.   Restrictions on BIT resources in items of hardware size, weight and power, memory size and test time.

k.   Requirement for BIT hardware reliability.

l.   Requirement for automatic error recovery.

m.   Requirement for fault detection consistency between hardware levels and maintenance levels.

Figure 5. Model requirements, system specification.

or other document for contract compliance (Subtask 201.2.6). This subtask is necessary to assure that system specification or contract parameters include only those parameters which the performing activity can control through design and support system development. The support burden and other effects of the government furnished material, administrative and logistic delay times, and other items outside the control of the performing activity must be accounted for in this process.

50.5.7 <u>Testability requirements for system specification.</u> Quantitative testability requirements are derived from the tradeoff analysis during the D&V phase and are incorporated in the system specification. Requirements may be expressed in terms of goals and thresholds rather than as a single number. Model requirements for testability in a system specification are provided in Figure 5 and are discussed below.

The system specification includes testability requirements for failure detection, failure isolation and BIT constraints. Requirement (a) defines the interface between the prime system and an external monitoring system, if applicable. Particular attention should be given to the use of BIT circuitry to provide performance and status monitoring. Requirement (b) provides the basis for all subsequent test design and evaluation. Failure modes are characterized based upon the component technology used, the assembly process used, the detrimental environment effects anticipated in the intended application, etc. Maximum use should be made of prior reliability analysis and fault analysis data such as FMEA and fault trees. The data represent a profile of estimated system failures to be constantly refined and updated as the design progresses.

Requirements (c) through (e) deal with test approaches. Requirement (c) permits the use of all test resources and, as such, should always demand 100% failure coverage. Requirement (d) indicates the proportion of failures to be detected automatically. Excluded failures form the basis for manual troubleshooting procedures (swapping large items, manual probing, etc.). Requirement (e) is a requirement for dealing quickly with critical failures and is a subset of (d). The failure detection approach selected is based upon the requirement for maximum acceptable failure latency. Concurrent (continuous) failure detection techniques (utilizing hardware redundancy, such as parity) are specified for monitoring those functions which are mission critical or affect safety and where protection must be provided against the propagation of errors through the system. The maximum permitted failure latency for concurrent failure detection and other classes of automatic testing is imposed by requirement (f). This requirement determines the frequency at which periodic diagnostic software, etc. will run. The frequency of periodic and on-demand testing is based upon function, failure rates, wear out factors, maximum acceptable failure latency, and the specified operational and maintenace concept.

Requirement (g) is the maximum BIT false alarm rate. Alarms which occur during system operation but cannot be later duplicated may actually be intermittent failures or may indeed be a true problem with the BIT circuitry. It may be useful to use the system specification to require sufficient instrumentation in the system to allow the sorting out and correction of real BIT problems (e.g., BIT faults, wrong thresholds, etc.) during operational test and evaluation.

Requirement (h) requires fault isolation by BIT to a subsystem or to a lower level part, depending upon the maintenance concept. This requirement is usually

expressed as "fault isolation to one item X% of the time, fault isolation to N or fewer items Y% of the time." Here, the total failure population (100%) consists of those failures detected by BIT (requirement (d)). The percentages should always be weighted by failure rates to accurately reflect the effectiveness of BIT in the field.

Requirement (i), fault isolation time, is derived from maintainability requirements, primarily Mean Time to Repair (MTTR) or repair time at some percentile.

Fault isolation time = repair time – (preparation time + disassembly time + interchange time + reassembly time + alignment time + verification time)

The preparation time, disassembly time, interchange time, reassembly time and alignment time may be estimated. The verification time is usually equal to the failure detection test time in that the same tests are likely to be used for each.

Requirement (j), BIT constraints, should not be arbitrarily imposed but should be consistent with the BIT performance specified in requirements (a) through (i). Historically, systems have needed about 5 to 20% additional hardware for implementations of adequate BIT. However, for some systems, 1% may be sufficient whereas other systems may need more than 20%.

Requirement (k), BIT reliability, again should not be arbitrarily imposed but should be consistent with the required BIT performance. This requirement may also be used to specify those critical functions for which a failed BIT must not interfere.

50.5.8 <u>Testability requirements for item specifications.</u> Testability requirements for configuration items (CIs) support two distinct requirements: system test (primarily BIT) and shop test (ATE and GPETE). Model requirements for testability are presented in Figure 6.

50.5.8.1 <u>System test.</u> Quantitative testability requirements for each CI are allocated from system testability requirements based upon relative failure rates of CIs, mission criticality of CIs or other specified criteria. In many digital systems, BIT is implemented, in whole or in part, through software. Here testability requirements will appear in a computer program configuration item (CPCI) development specification. The program may be dedicated to the BIT function (i.e., a maintenance program) or may be a mission program which contains test functions.

50.5.8.2 <u>UUT test.</u> Shop test requirements are determined by how the CI is further partitioned, if at all, into UUTs. Testability requirements for each UUT should be included in the appropriate CI development specification.

50.6 <u>Task 202 – Testability preliminary design and analysis</u>

50.6.1 <u>Scope of testability design.</u> Testability addresses three major design areas:

a.   The compatibility between the item and its off-line test equipment

The following CI requirements are allocated from system requirements:

a. Definition of fault modes to be used as the basis for test design.

b. Requirement for fault coverage using full test resources (Note: Requirement should be 100% fault coverage).

c. Requirement for fault coverage and failure reporting using full BIT resources of CI.

d. Requirement for fault coverage and failure reporting using only BIT monitoring of operational signals within CI.

e. Requirement for maximum failure latency for BIT and operational monitoring of critical signals.

f. Requirement for maximum BIT false alarm rate. Include criteria for reporting a transient or intermittent fault as a valid BIT alarm.

g. Requirement for fault isolation to one or more numbers of subitems using CI BIT.

h. Requirement for CI fault isolation times using BIT.

i. Restrictions on BIT resources.

j. Requirement for BIT hardware reliability.

k. Requirement for periodic verification of calibration of BIT sensors.

The following requirements apply to each partition within the configuration item which is identified as a UUT:

a. Requirements for compatibility (functional, electrical, mechanical) between the UUT and the selected ATE.

b. Requirements for test point access for the UUT.

c. Requirements for fault coverage using full test resources of the intermediate or depot maintenance facilities. (Note: Requirement should be 100% fault coverage).

d. Requirement for fault coverage using automatic test resources (ATE and TPS plus embedded BIT).

e. Requirement for average (or maximum) test time for GO/NO GO tests using automatic test resources.

f. Requirement for maximum rate of false NO GO indications resulting in cannot duplicates and retest okays using automatic test resources.

g. Requirement for fault isolation to one or more number of subitems within the UUT using automatic test resources.

h. Requirement for fault isolation times using automatic test resources.

NOTE: A UUT at an intermediate maintenance facility may contain several smaller UUTs to be tested at a depot maintenance facility and all should be listed in the CI specification.

Figure 6. Model requirements, CI development specification.

     b.   The BIT (hardware and software) provided in the item to detect and isolate faults

     c.   The *structure of the item* in terms of **(1)** partitioning to enhance fault isolation and **(2)** providing access and control to the tester (whether BIT or off-line test) for internal nodes within the item to enhance fault detection and isolation.

     Testability concepts, when applied to weapon system and support system designs, have the potential to:

     a.   Facilitate the development of high quality tests

     b.   Facilitate manufacturing test

     c.   Provide a performance monitoring capability (through BIT)

     d.   Facilitate the development of fault isolation procedures for technical manuals

     e.   Improve the quality and reduce the cost of maintenance testing and repair at all levels of maintenance.

Subtask 202.2.1 requires the performing activity to integrate testability into the design process. Several design guides and handbooks are available which explain testability design techniques which have proven successful in certain applications. (See Section 20, publications). The following paragraphs provide a summary of some testability design issues.

50.6.2   <u>D&V system design.</u>   During the D&V phase,alternate system designs are evaluated. This includes the analysis of manpower requirements, support costs, reliability, maintainability, and system readiness. There are usually no detailed, quantitative specifications for testability in D&V system designs. In fact, the purpose of the D&V phase, with respect to testability, is to determine quantitative testability requirements that are achievable, affordable, and adequately support system operation and maintenance. In making this determination, it is reasonable to apply Task 202 to selected items to be implemented in the alternative systems. These items may be selected because they have potential testing problems or are not expected to be modified during FSD.

50.6.3   <u>Test design tradeoffs.</u>   The overall test design will usually incorporate a mix of BIT, off-line automatic test and manual test which provides a level of test capability consistent with operational availability requirements and life-cycle cost requirements. Alternate designs are analyzed and traded off against requirements of performance, supportability, and cost to arrive at a configuration best meeting the requirements at minimum cost.

     a.   <u>Manual or automatic test tradeoffs.</u>   Decisions regarding the type of test equipment to be used for system monitoring and maintenance are made based upon repair policies, overall maintenance plans and planned number of systems. Tradeoffs are

made for test requirements at each maintenance level, considering test complexity, time to fault isolate, operational environment, logistic support requirements, development time and cost. The degree of testing automation must be consistent with the planned skill levels of the equipment operators and maintenance personnel.

   b.   BIT or ATE tradeoffs.   Within the category of automatic testing, the allocation of requirements to BIT or off-line test is driven by the natural differences between BIT capabilities and ATE capabilities:

   1.   BIT is used to provide initial fault detection for a system or equipment and to provide initial fault isolation to a small group of items.   BIT has the advantage of operating in the mission environment and being self-sufficient.

   2.   Off-line ATE is used to provide fault detection for an item as a UUT and provide fault isolation to components within an item. ATE does not impose the weight, volume, power and reliability penalties on the prime system that BIT does.

   c.   Coordination.   In developing off-line test designs, maximum utilization should be made of available BIT capability within each UUT. In addition, test tolerances used by off-line test should be tighter than those used by BIT to avoid the "retest okay" problem.

   50.6.4   General testability issues.   Testability features in a system or item design support both BIT and off-line test.

   a.   Physical partitioning.   The ease or difficulty of fault isolation depends to a large extent upon the size and complexity of replaceable items:

   1.   The physical partitioning of a system into items should be based, in part, upon the enhancement of the fault isolation process.

   2.   The maximum number of item pins must be consistent with the interface capabilities of the proposed ATE.

   3.   Items should be limited to only analog or only digital circuitry, whenever practical, and when functional partitioning is not impaired.

   4.   Where practical, circuits belonging to an inherently large ambiguity group due to signal fan-out should be placed in the same package.

   b.   Functional partitioning.   Whenever possible, each function should be implemented on a single replaceable item to make fault isolation straightforward. If more than one function is placed on a replaceable item, provisions should be made to allow for the independent testing of each function.

c. **Electrical partitioning.** Whenever possible, the block of circuitry currently being tested should be isolated from circuitry not being tested through the use of blocking gates, tri-state devices, relays, etc. This "divide and conquer" approach is based upon the concept that test time increases exponentially with the complexity of the circuit.

d. **Initialization.** The system or equipment should be designed such that it has a well-defined initial state to commence the fault isolation process. Non-achievement of the correct initial state should be reported to the operator along with sufficient signature data for fault isolation. The system or equipment should be designed to initialize to a unique state such that it will respond in a consistent manner for multiple testing of a given failure.

e. **Module interface.** Maximum use should be made of available connector pins to incorporate test control and access. For high density circuits and boards, preference may be given to additional circuitry (e.g., multiplexers, shift registers) rather than additional pins.

f. **Test control (controllability).** Special test input signals, data paths, and circuitry should be incorporated to provide the test system, whether BIT or ATE, sufficient control over internal item or component operation for the detection and isolation of internal faults. Special attention is given to the independent control of clock lines, clear lines, breaking of feedback loops, and tri-state isolation of components.

g. **Test access (observability).** Test points, data paths, and circuitry should be incorporated to provide the test system, whether BIT or ATE, sufficient signature data for fault detection and isolation within the item. The selection of physical (real) test points should be sufficient to accurately determine the value of internal nodes (virtual test points) of interest. There should be no requirement to probe internal points for organizational-level fault isolation.

h. **Parts selection.** In selecting between parts, each with satisfactory performance characteristics, preference is given to integrated circuit components and assembled items which have satisfactory testability characteristics. Preference is given to those integrated circuits for which sufficient disclosure of internal structure and failure modes has been provided as a basis for effective, economical testing.

i. **Failure mode characterization.** Test design and testability design features which support testing should be based upon expected failure modes and effects. Failure modes (e.g., stuck faults, open faults, out-of-tolerance faults) must be characterized based upon the component technology used, the assembly process used and the detrimental environment effects anticipated in the intended application. Maximum use is made of prior analysis and government data.

50.6.5 **UUT and ATE compatibility.** Each UUT should be designed such that it is electrically and mechanically compatible with selected or available ATE so as to reduce or eliminate the need for a large number of unique interface device designs. If the ATE has not been selected, the general compatibility requirements of MIL-STD-2076 may be applied to the UUT and ATE design as appropriate.

a. Electrical partitioning for off-line test. The ATE should have sufficient control over the electrical partitioning of the UUT such that relatively small, independent, and manageable blocks of circuitry may be defined as the basis of test derivation, test documentation, and test evaluation. The UUT design should support running individual test program segments on an ATE independent of other test program segments.

b. UUT test point selection. The number and placement of UUT test points is based upon the following:

1. Test points are selected based upon fault isolation requirements.

2. Test points selected are readily accessible for connection to ATE via system/equipment connectors or test connectors.

3. Test points are chosen so that high voltage and current measurements are consistent with safety requirements.

4. Test point measurements relate to a common equipment ground.

5. Test points are decoupled from the ATE to assure that degradation of equipment performance does not occur as a result of connections to the ATE.

6. Test points of high voltage or current are physically isolated from test points of low logic level signals.

7. Test points are selected with due consideration for ATE implementation and consistent with reasonable ATE frequency requirements.

8. Test points are chosen to segregate analog and digital circuitry for independent testing.

9. Test points are selected with due consideration for ATE implementation and consistent with reasonable ATE measurement accuracies.

50.6.6 Built-in test. Suitable BIT features are incorporated into each item to provide initial fault detection and fault isolation to a subitem. This BIT may also be utilized to verify the operability of the system following a corrective maintenance action or a reconfiguration into a degraded mode.

a. BIT fault detection approaches. Fault detection approaches may be categorized as concurrent (continuous), monitoring, periodic, and on-demand techniques. The selection is based upon the requirement for maximum acceptable fault latency. Concurrent (continuous) fault detection techniques (utilizing hardware redundancy) are used for monitoring those functions which are mission critical or affect safety and where

protection must be provided against the propagation of errors through the system. *Periodic testing is used for monitoring those functions which provide backup or standby* capabilities or are not mission critical. On-demand testing is used for monitoring those functions which require operator interaction, sensor simulation, and so forth, or which are not easily, safely, or cost-effectively initiated automatically. The frequency and length of periodic and on-demand testing is based upon function, failure rates, wear out factors, maximum acceptable failure latency, and the specified maintenance concept.

b. Electrical partitioning for BIT. The BIT circuitry should have sufficient control over the electrical partitioning of the item such that relatively small, independent, and manageable blocks of circuitry can be defined as the basis of test derivation, test documentation, and test evaluation. In particular, for computer-based equipment, such control should be made available to BIT software.

c. BIT design tradeoffs. Some of the BIT design tradeoff issues are listed below:

1. Centralized versus distributed BIT.
2. Tailored versus flexible BIT.
3. Active stimulus versus passive monitoring.
4. Circuitry to test BIT circuitry.
5. Hardware versus software versus firmware BIT.
6. Placement of BIT failure indicators.

50.6.7 BIT software. BIT software includes confidence tests (GO/NO GO tests) for fault detection and diagnostic tests for fault isolation.

a. BIT memory sizing. When estimating memory requirements for a digital system, it is essential that sufficient words are reserved:

1. In control memory for the storage of micro-diagnostics and initialization routines.

2. In main memory for the storage of error processing routines and confidence tests.

3. In secondary memory (e.g., disk memory) for the storage of diagnostic routines.

In addition, the width of each memory word should be sufficient to support BIT requirements:

1. In control memory to achieve controllability of hardware components.

2. In main and secondary memory to provide for error detection and error correction techniques, as required.

Finally, it is important that a sufficient number of memory words are assigned to non-alterable memory resources (e.g., read only memory, protected memory areas) to ensure the integrity of critical test routines and data. Sufficient hardware and software redundancy should exist to confidently load critical software segments.

b. **Application software test provisions.** The system application software (mission software) should provide for timely detection of hardware faults. The application software design should include sufficient interrupt and trap capability to support the immediate processing of errors detected by concurrent BIT hardware prior to the destruction of data bases or loss of information concerning the nature of the error. The operating system and each critical application program must contain software checks sufficient to meet failure latency requirements.

c. **Application software error processing.** Error processing routines in the application software invoked by interrupts and traps should be designed with the full participation of hardware design and test engineers. The processing to be performed (re-entry, automatic error correction, diagnostic call, operator message, error logging, immediate halt, etc.) must be consistent with the failure modes and effects analysis. The operating system hierarchy should be designed to allow the diagnostic software sufficient control and observation of hardware components.

50.6.8 **System-level Built-in test.** System BIT includes a mix of BIT hardware, BIT software, and application software error checks to provide the required degree of fault detection and isolation at the system level.

a. **BIT intermittent failure detection.** System BIT must be designed to respond in a predictable manner to intermittent failures, considering both the maximizing of safety and the minimizing of BIT alarms. Detection of a failure by BIT should be followed by a second test of the failing operation, whenever practical. The numbers of repeated tests and repeated failures necessary to establish a solid fault condition needs to be determined. Conditions under which the operator is to be notified of recoverable intermittent failures should be determined, based upon failure criticality, frequency of concurrence, and trends. For digital systems, failure data may be recorded in a failure history queue. Data from the failure history queue could be made accessible to assist in troubleshooting of intermittent failures and to identify hardware which is trending toward solid failure. The initial implementation of system BIT should be flexible. For example, test tolerances may be stored in software or firmware so that the tolerances and filtering algorithms may be easily changed if BIT is generating too many false alarms.

b. **BIT failure location.** Suitable BIT features must be incorporated into the system to localize failures to a small number of items and to advise operator personnel of degraded mode options. In some cases, the BIT may need to isolate a failure to a level lower than a replaceable item in order to determine what system functions are lost and which system functions are operational. When subsystems are to be developed by subcontractors, each subsystem specification should contain a requirement for self-contained test with minimal reliance upon the system contractor to perform detailed testing of each subsystem through system-level test. The interface between system and

subsystem test should be straightforward and relatively simple (e.g., test initiate, test response, test signature). This allows for the evaluation and demonstration of BIT quality for each subcontractor prior to system integration.

c. _Fault-tolerant design coordination._ If system availability or safety requires continued system operation in the presence of certain faults, then the fault-tolerant design and testability design efforts should be closely coordinated. Equipment redundancy or functional redundancy may be used to assist in testing. Fault assessment, reconfiguration into degraded mode, and configuration verification should make maximum use of testing resources. The design should provide for the independent testing of redundant circuitry.

50.6.9 _Application of testability measures._ Testability achievement is tracked through system design, production and in-service use utilizing the measures listed in Table III, or similar measures, as appropriate to the phase of system development. Table III provides general guidance on applicability of measures and is subdivided into three basic areas:

a. _Inherent (design) measures._ Inherent testability measures are evaluations of testability dependent only upon item design characteristics. The evaluation identifies the presence or absence of hardware features which support testing and identifies general problem areas. The analysis primarily serves as feedback to the performing activity at a point in time when the design can be changed relatively easily. (See 50.6.10 and 50.6.11)

b. _Test effectiveness measures._ Test effectiveness measures are evaluations of testability dependent upon item design, its relationship to the chosen maintenance environment and the testing capability of that environment. (See 5.7.3-.5)

c. _In-service measures._ In-service testability measures are evaluations of testability based upon measurable field (i.e., operational) experience. (See 5.7.6)

5.6.10 _Qualitative inherent testability evaluation._ Subtask 202.2.3 requires that the performing activity gives early visibility to testability issues and shows, in a qualitative manner, that the testability considerations have been included in the preliminary design. Testability considerations include, as a minimum, those concepts described in 5.6.4 through 5.6.7.

50.6.11 _Inherent testability assessment._ Subtask 202.2.3 requires that the inherent ability of an item to support high quality testing be assessed using Appendix B.

50.6.11.1 _Preliminary design activities._ The performing activity prepares a checklist of testability-related design issues which are relevant to the design, and proposes a method of quantitatively scoring the degree of achievement of testability for each design issue. A checklist is to be prepared for each item specified by the requiring authority. Each checklist is tailored to the design characteristics of the item. The procuring authority reviews the checklist and the scoring criteria and either concurs or negotiates changes. The checklist approach allows for "structured" testability design

Table III. Testability Measure Application Guidance Matrix

Testability Measure	Preliminary Design	Detail Design	Build/ Demonstration	Production/ Deployment
Inherent	X	X		
Test Effectiveness				
Functional coverage	X	X	X	
Predicted FD/FI		X	X	
Predicted FD/FI times		X	X	
Predicted test cost	X	X	X	
In-service				
Achieved FD/FI				X
Achieved FI time				X
FA/CND/RTOK rates				X
Actual test cost				X
FD/FI	Fault detection and fault isolation			
FA/CND/RTOK	False alarm, cannot duplicate and retest okay			

approaches, such as scan path, to receive a high score simply because of their inclusion in the design. The checklist should be finalized prior to the preliminary design review.

50.6.11.2 Checklist scoring. As the design progresses, each checklist issue is examined and scored for testability compliance. The use of objective, automated testability analysis tools (e.g., SCOAP, STAMP) for scoring is permitted. The scores are weighted and summed, giving a single inherent testability figure of merit for the design. The design for testability process continues until the figure of merit reaches a predetermined threshold value.

50.6.11.3 Threshold determination. The requiring authority must assign a threshold value to be used for the inherent testability assessment. Due to the wide variety of possible items which may be analyzed, a single "best" threshold value cannot be recommended although a value in the range of 80 to 90 should force proper attention to the assessment process. The actual value chosen is not all that critical since another degree of freedom is available through the negotiation of weighting factors after the threshold is established. In fact, since each checklist issue is weighted according to its perceived importance in achieving a testable design, both the eventual design and the eventual meeting of the overall figure of merit criteria are essentially determined by the requiring authority's concurrence on the issues to be included and the scoring for each issue. It is incumbent upon the requiring authority to be aware of the importance of each proposed issue in achieving a testable design.

50.7 Task 203 – Testability detail design and analysis

50.7.1 Testability design techniques. During detail design, the testability design techniques of the preliminary design are further refined and implemented. Guidance provided in 50.6.3 through 50.6.8 for preliminary design applies equally to detail design.

50.7.2 Inherent testability assessment. During detail design, Appendix B may be applied to the evolving design. Guidance provided in 50.6.10 and 50.6.11 for preliminary design applies equally to detail design. The inherent testability assessment should be completed prior to the critical design review.

50.7.3 Test effectiveness measures. At the completion of system or equipment design, test sequences should be generated for that design and test effectiveness measured. Analysis need not wait for the completion of TPSs or BIT software. The use of models (50.7.4) is encouraged since they can analyze test effectiveness on a large number of postulated faults (approaching 100% of the specified failure population) prior to incorporating the test stimulus in a test language (e.g., ATLAS) or embedded computer language. The results of the analysis can feed forward to influence TPS or BIT software design and feed back to influence redesign of the prime item to improve its testability. The identification of undetected or poorly isolated failures can lead to three actions:

    a.   The failure is not detectable by any test sequence. Any failures, such as those in unused circuitry, which are impossible to detect are deleted from the failure population.

b. The failure is potentially detectable, but the test sequence is deficient.
Additional stimulus patterns are added to the test sequence.

c. The failure is potentially detectable, but the item's hardware design
precludes the use of a test sequence of reasonable length or complexity.
The prime item is redesigned to provide additional test control, test
access, or both.

Test effectiveness measures include functional coverage (an enumeration of which
functions in an item are exercised by a test), failure-based measures as described below,
and cost or benefit measures (50.7.5).

50.7.3.1 <u>Fault coverage.</u> Fault detection coverage (FD) is calculated as follows:

$$FD = \frac{\lambda_d}{\lambda} \qquad \text{where}$$

$$d = \sum_{i=1}^{K} \lambda_i,$$

where λ_i is the failure rate of the ith detected failure, λ is the overall
failure rate, and K is the number of detected failures.

50.7.3.2 <u>Fault resolution.</u> To calculate predicted fault resolution, data are required
which correlate each detected failure with the signature it produces during testing. The
data are most conveniently ordered by signature and by failed module within each
signature (fault dictionary format).

N   =   number of unique signatures in dictionary (number of unique test
responses)

i   =   signature index

M_i =   number of modules listed in signature i

j   =   module index within signature

λ_{ij} =   failure rate for jth module for failures providing signature i

λ_d =   overall failure rate of detected failures = $\displaystyle\sum_{i=1}^{N} \sum_{j=1}^{M_i} \lambda_{ij}$

FR_L =   Fault Resolution to L or fewer modules (% replacements with
ambiguity $\leq$ L)

If all modules under a signature are replaced as a block:

$$FR_L = \frac{100}{\lambda_d} \sum_{i=1}^{N} X_i \sum_{j=1}^{M_i} \lambda_{ij} \qquad \text{where } X_i = \begin{cases} 1 \text{ if } M_i \leq L \\ 0 \text{ if } M_i > L \end{cases}$$

If detailed failure rate information is unavailable or unreliable, or it is desired to consider each fault as having equal probability, the above equation reduces to:

$$FR_L = \frac{100}{K} \sum_{i=1}^{N} X_i M_i \qquad \text{where } K = \text{number of detected}$$

$$\text{faults} = \sum_{i=1}^{N} M_i$$

If each of the L modules under the signature group is replaced, in turn, and the test rerun for PASS or FAIL:

$$FR_L = \frac{100}{\lambda_d} \sum_{i=1}^{N} \sum_{j=1}^{L} \lambda_{ij} \qquad \text{where } \lambda_{ij} = 0 \text{ if } j > M_i$$

50.7.3.3 <u>Fault detection time</u>. Fault detection time (or failure latency) is the time which elapses between the occurrence of a fault and the detection (reporting) of the fault by the test process. This measure is most useful in characterizing how BIT deals with critical failures. A suggested format is shown in the following example:

	% of Class	Max. detection time
Failure class 1 (most critical)	95%	≤ 1 second
	100%	≤ 1 minute
Failure class 2 (critical)	85%	≤ 1 minute

This measure requires the enumeration of signals considered most critical, critical, and so forth and an estimation made of the worst case failure latency for each signal.

50.7.3.4 <u>Fault isolation time</u>. During maintenance actions using BIT or off-line test, the time to fault isolate is often the largest and most unpredictable element of repair time. The testability program should not only attempt to reduce the fault isolation time but should also try to provide accurate predictions of fault isolation times to maintenance planners per Task 205 of MIL-STD-470A. The fault isolation time may be expressed as an average time, a maximum time (at some percentile), or both. The time is based not only on the length of the diagnostic test sequence but also must include an estimation of time required for any manual intervention (e.g., the use of a sequential substitution fault isolation procedure).

50.7.4 <u>Fault modeling</u>. The physical insertion of a sufficient number of faults into an item to determine its response to a test sequence has some obvious problems. The two most serious problems are that the time and expense of inserting even a small number of representative faults into the item is prohibitive and the ability to insert

representative faults is limited by circuit packaging. A computer program may be used to inject (through software) a large number of faults into a software model of the hardware item. The same program can simulate the behavior of an item containing one of the faults in response to the stimulus. The test stimulus may then be evaluated in terms of fault detection and fault resolution based upon a large number of fault cases. Computer programs are well established as tools to simulate the fault behavior of digital circuits and grade digital tests for Test Program Set development. These same programs may be used to grade built-in tests using bootstrap sequences, microdiagnostics, BIT software patterns, etc. as test stimulus. In addition, several programs automatically generate test sequences for the simulator to grade. An example of this is the Hierarchical Interactive Test Simulator (HITS) program. Programs are also available to simulate the fault behavior of analog circuits, but the test stimuli must be provided manually. The usefulness of this approach depends upon the ability of the models (item models and fault models) to accurately reflect actual operation and actual field failures. The item must be modeled at a level of detail which allows all important failure modes to be included. The fault-free behavior of the item model must be validated prior to modeling faults by applying a functional test and comparing the modeled response to the expected response or to the response of a known good hardware item.

50.7.5 System level test effectiveness. The level of BIT fault detection for the overall system is calculated as:

$$FD = \frac{\sum \lambda_i FD_i}{\sum \lambda_i} \qquad i = 1 \text{ to number of items}$$

where λ_i is the failure rate of the ith item and FD_i is the fault detection prediction for the i th item. This applies equally for systems with centralized BIT and systems with distributed BIT (i.e., BIT in each item).

50.7.6 Testability cost and benefit data. Ultimately, all test performance measures translate into cost impacts. Higher quality tests usually cost more to produce but should result in cost savings over the life cycle of the system. These cost data are critical in setting reasonable testability requirements within the framework of supportability analysis. Subtask 203.2.7 ensures that testability cost data for this acquisition program are available for incorporation into appropriate data bases for use by future supportability analysis efforts.

a. **Non-recurring costs.** The development costs associated with the incorporation of testability into the system or equipment include, but are not limited to, the following:

1. Testability program planning costs
2. Testability design costs
3. Testability modeling and analysis costs
4. Testability data preparation costs.

b. **Recurring costs and penalties.** The production, operation and maintenance costs and penalties associated with the incorporation of testability into the system or equipment include, but are not limited to, the following:

1. Per item costs of additional hardware required for BIT and testability capabilities.
2. Volume and weight required for additional hardware, additional connectors, and increased modularity.
3. Power required for additional hardware.
4. Computer memory required for BIT software.
5. Possibility of system interruption due to failure within BIT circuitry.
6. Reliability impact due to additional hardware.

c. Benefit assessment, development and production. The impact of testability on development and production costs includes, but is not limited to, the following:

1. Test generation costs
2. Production test costs
3. Test equipment costs
4. Interface device costs

d. Benefit assessment, operation and maintenance. The impact (actual or predicted) of testability on operation and maintenance costs includes, but is not limited to, the following:

1. Test and repair costs
2. Test and repair time
3. Manpower costs
4. Training costs
5. Spares cost

50.7.7 In-service testability measures. In-service testability measures evaluate the impact of actual operational and maintenance environments on the ability of production systems and equipments to be tested. The planning for the collection of data to measure test effectiveness in the operational and maintenance environment is accomplished through Task 103. It is important to realize that testing problems in the field may be corrected in many ways (e.g., personnel changes, organizational changes, procedural changes, etc.) and do not always result in engineering design changes. In-service testability measures include:

a. Level of automation. Are the testing tools provided consistent with the training/skill levels of assigned personnel?

b. BIT fault detection. Does BIT provide timely and accurate detection of faults so as to minimize reliance on manual detection (e.g., squawks)?

c. BIT false alarm rate. Are BIT false alarms adversely impacting operational availability and maintenance workloads?

d.   Retest okay. Are faults detected at one level of maintenance also detected at the next level of maintenance?

e.   BIT fault isolation time. Does BIT support system MTTR and system availability requirements?

f.   Off-line fault isolation time. Does ATE and its associated TPSs support shop throughput requirements?

g.   Fault resolution. Does poor fault resolution for BIT or ATE adversely impact spares availability?

h.   BIT reliability. Is poor BIT reliability adversely impacting the mission?

50.8   Task 301 - Testability demonstration

50.8.1   Demonstration parameters. It is useful to distinguish between fault detection and isolation at the system level (organizational maintenance level) and fault detection and isolation performed off-line (higher maintenance levels). The former may be demonstrated as part of a standard maintainability demonstration if certain testability concerns (Subtask 301.2.1) are incorporated into the maintainability demonstration plans and procedures. The latter may be demonstrated as part of the evaluation procedures for Test Program Sets, including evaluation of software, interfaces and documentation.

50.8.2   BIT and off-line test correlation. Through the development of the testability demonstration plan, the items to be demonstrated under the maintainability demonstration and the TPS demonstration may be coordinated (e.g., some common faults to be inserted) so as to provide data on the correlation of BIT results and off-line test results. This can give an early indication of possible "cannot duplicate" (CND) problems in the field.

50.8.3   BIT false alarm rate. One important testability parameter, BIT false alarm rate, is difficult to measure in the controlled environment of a demonstration procedure. If the false alarm rate was relatively high, it would be possible to make use of a reliability demonstration procedure from MIL-STD-781 to demonstrate the false alarm rate, treating each BIT false alarm as a relevant failure. The environmental conditions during the demonstration should be indicative of the expected operational environment in order to experience a wide range of false alarm causes.

50.8.4   Model validation. Even with a reasonably large sample of inserted faults, a demonstration can yield only limited data on actual test effectiveness. However, a demonstration is also useful in validating some of the assumptions and models that were used during the earlier testability analysis and prediction efforts (Task 203) which were based upon a much larger fault set. If certain assumptions or models are invalidated by the demonstration, appropriate portions of Task 203 should be repeated and new predictions should be made.

10. SCOPE

10.1 Purpose. This appendix provides requirements for the assessment of the inherent testability of system or equipment design.

10.2 Application. Appendix B shall be considered as forming a part of the standard.

20. REFERENCED DOCUMENTS

Not applicable.

30. DEFINITIONS

Not applicable.

40. GENERAL REQUIREMENTS

40.1 General. Conduct an analysis of the inherent (intrinsic) testability of the design. The analysis identifies the presence or absence of hardware features which support testing and identifies problem areas. The method of this Appendix shall be applied to each item identified for Inherent Testability Assessment by the requiring authority. The data required by this appendix shall be determined by the performing activity and approved by the requiring authority. Any testability criteria designated as mandatory by the requiring authority, and therefore not subject to design tradeoffs, should be assessed separately from this procedure.

50. DETAILED REQUIREMENTS

50.1 Procedure. Assess the inherent testability of the system or equipment design using the Inherent Testability Checklist, Table IV.

    a. Delete those testability criteria from Table IV which are not applicable to the design.

    b. Add additional testability criteria to Table IV which are relevant to the design (or modify original criteria).

    c. Assign weighting factors (WT) to each item based upon its relative importance in achieving a testable product. $(1 \leq WT \leq 10)$

    d. Develop a scoring system for item $(0 \leq score \leq 100)$ where 100 represents maximum testability and 0 represents a complete lack of testability.

    e. Obtain concurrence on (a) through (d) above from the requiring authority.

f.   Count the design attributes which are relevant to each testability item (e.g., the total number of nodes in a circuit).

g.   Count the design attributes which meet the testability criteria for each item (e.g., the number of nodes accessible to the tester).

h.   Apply the scoring system to each item (e.g., Score = accessible nodes ÷ total nodes, or Score = 100 if YES and = 0 if NO).

i.   Calculate the weighted score for each item, WT Score = WT x Score.

j.   Calculate the inherent testability of the design, TESTABILITY = Sum (WT Score) ÷ Sum (WT).

50.2   **Criteria.** Modify the design as necessary until the inherent testability equals or exceeds the threshold value.

Table IV. Inherent Testability Checklist

	WT	Total Number	Number Meeting Criteria	Score	WT Score
Mechanical Design					
Is a standard grid layout used on boards to facilitate identification of components?					
Is enough spacing provided between components to allow for clips and test probes?					
Are all components oriented in the same direction (pin 1 always in same position)?					
Are standard connector pin positions used for power, ground, clock, test, etc., signals?					
Are the number of input and output (I/O) pins in an edge connector or cable connector compatible with the I/O capabilities of the selected test equipment?					
Are connector pins arranged such that the shorting of physically adjacent pins will cause minimum damage?					
Is defeatable keying used on each board so as to reduce the number of unique interface adapters required?					
When possible, are power and ground included in the I/O connector or test connector?					
Have test and repair requirements impacted decisions on conformal coating?					
Is the design free of special set-up requirements (e.g., special cooling) which would slow testing?					

	WT	Total Number	Number Meeting Criteria	Score	WT Score

Mechanical Design (cont'd)

- Does the item warm up in a reasonable amount of time?

. Is each hardware component clearly labelled?

Partitioning

Is each function to be tested placed wholly upon one board?

If more than one function is placed on a board, can each be tested independently?

Within a function, can complex digital and analog circuitry be tested independently?

Within a function, is the size of each block of circuitry to be tested small enough for economical fault detection and isolation?

If required, are pull up resistors located on same board as the driving component?

Are analog circuits partitioned by frequency to ease tester compatibility?

Is the number of power supplies required compatible with the test equipment?

: Is the number and type of stimuli required compatible with the test equipment?

. Are elements which are included in an ambiguity group placed in the same package?

Test Control

Are unused connector pins used to provide test stimulus and control from the tester to internal nodes?

WT	Total Number	Number Meeting Criteria	Score	WT Score

Test Control (cont'd)

Can circuitry be quickly and easily driven to a known initial state? (e.g., master clear, less than N clocks for initialization sequence)?

Are redundant elements in design capable of being independently tested?

Is it possible to disable on-board oscillators and drive all logic using a tester clock?

Can long counter chains be broken into smaller segments in test mode with each segment under tester control?

Can the tester electrically partition the item into smaller independent, easy-to-test segments? (e.g., placing tri-state elements in a high impedance state).

Is circuitry provided to by-pass any (unavoidable) one-shot circuitry?

Can feedback loops be broken under control of the tester?

In microprocessor-based systems, does the tester have access to the data bus, address bus and important control lines?

Are test control points included at those nodes which have high fan-in (i.e., test bottlenecks)?

Are input buffers provided for these control point signals with high drive capability requirements?

Are active components, such as demultiplexers and shift registers, used to allow the tester to control necessary internal nodes using available input pins?

Test Access

- Are unused connector pins used to provide additional internal node data to the tester?

- Are signal lines and test points designed to drive the capacitive loading represented by the test equipment?

Are test points provided such that the tester can monitor and synchronize to onboard clock circuits?

Are test access points placed at those nodes which have high fan-out?

Are buffers employed when the test point is a latch and susceptible to reflections?

Are buffers or divider circuits employed to protect those test points which may be damaged by an inadvertent short circuit?

Are active components, such as multiplexers and shift registers, used to make necessary internal node test data available to the tester over available output pins?

Are all high voltages scaled down within the item prior to providing test point access so as to be consistent with tester capabilities?

Is the measurement accuracy of the test equipment adequate compared to the tolerance requirement of the item being tested?

Parts Selection

Is the number of different part types the minimum possible?

WT	Total Number	Number Meeting Criteria	Score	WT Score

WT	Total Number	Number Meeting Criteria	Score	WT Score

Parts Selection (cont'd)

Have parts been selected which are well characterized in terms of failure modes?

Are the parts independent of refresh requirements? If not, are dynamic devices supported by sufficient clocking during testing?

Is a single logic family being used? If not, is a common signal level used for interconnections?

Analog Design

Is one test point per discrete active stage brought out to the connector?

Is each test point adequately buffered or isolated from the main signal path?

Are multiple, interactive adjustments prohibited for production items?

Are functional circuits of low complexity? (Amplifiers, regulators, etc.)

Are circuits functionally complete without bias networks or loads on some other UUT?

Is a minimum number of multiple phase-related or timing-related stimulus required?

Is a minimum number of phase or timing measurements required?

Is a minimum number of complex modulation or unique timing patterns required?

Are stimulus frequencies compatible with tester capabilties?

Analog Design (cont'd)

Are stimulus rise time or pulse width requirements compatible with tester capabilities?

Does response measurements involve frequencies compatible with tester capabilities?

Are response rise time or pulse width measurements compatible with tester capabilities?

Are stimulus amplitude requirements within the capability of the test equipment?

Are response amplitude measurements within the capability of the test equipment?

Does the design avoid external feedback loops?

Does the design avoid or compensate for temperature sensitive components?

Does the design allow testing without heat sinks?

Are standard types of connectors used?

Digital Design

Does the design contain only synchronous logic?

Are all clocks of differing phases and frequencies derived from a single master clock?

Are all memory elements clocked by a derivative of the master clock? (Avoid elements clocked by data from other elements.)

WT	Total Number	Number Meeting Criteria	Score	WT Score

	WT	Total Number	Number Meeting Criteria	Score	WT Score

Digital Design (cont'd)

Does the design avoid resistance capacitance one-shots and dependence upon logic delays to generate timing pulses?

Does the design support testing of "bit slices"?

Does the design include data wraparound circuitry at major interfaces?

Do all buses have a default value when unselected?

For multilayer boards, is the layout of each major bus such that current probes or other techniques may be used for fault isolation beyond the node?

Is a known output defined for every word in a Read Only Memory (ROM)? Will the improper selection of an unused address result in a well defined error state?

Is the number of fan-outs for each internal circuit limited to a predetermined value?

Is the number of fan-outs for each board output limited to a predetermined value?

Are latches provided at the inputs to a board in those cases where tester input skew could be a problem?

Is the design free of WIRED-ORs?

Does the design include current limiters to prevent domino effect failures?

If the design incorporates a structured testability design technique (e.g., Scan Path, Signature Analysis), are all the design rules satisfied?

Digital Design (cont'd)

Are sockets provided for microprocessors and other complex components?

Built-in Test (BIT)

Can BIT in each item be exercised under control of the test equipment?

Is the Test Program Set designed to take advantage of BIT capabilities?

Are on-board BIT indicators used for important functions? Are BIT indicators designed such that a BIT failure will give a FAIL indication?

Does the BIT use a building-block approach (e.g., all inputs to a function are verified before that function is tested)?

Does building-block BIT make maximum use of mission circuitry?

Is BIT optimally allocated in hardware, software and firmware?

Does on-board ROM contain self-test routines?

Does BIT include a method of saving on-line test data for the analysis of intermittent failures and operational failures which are non-repeatable in the maintenance environment?

Is the failure rate contribution of the BIT circuitry within stated constraints?

Is the additional weight attributed to BIT within stated constraints?

Is the additional volume attributed to BIT within stated constraints?

WT	Total Number	Number Meeting Criteria	Score	WT Score

Built-in Test (BIT) (cont'd)

Is the additional power consumption attributed to BIT within stated constraints?

Is the additional part count due to BIT within stated constraints?

Does the allocation of BIT capability to each item reflect the relative failure rate of the items and the criticality of the items' functions?

Are BIT threshold values, which may require changing as a result of operational experience, incorporated in software or easily-modified firmware?

Is processing or filtering of BIT sensor data performed to minimize BIT false alarms?

Are the data provided by BIT tailored to the differing needs of the system operator and the system maintainer?

Is sufficient memory allocated for confidence tests and diagnostic software?

Does mission software include sufficient hardware error detection capability?

Is the failure latency associated with a particular implementation of BIT consistent with the criticality of the function ing monitored?

BIT threshold limits for each parame-
ined as a result of considering
eter's distribution statistics,
surement error and the
tection/false alarm char-

WT	Total Number	Number Meeting Criteria	Score	WT Score

	WT	Total Number	Number Meeting Criteria	Score	WT Score

Test Requirements

Has Level of Repair Analysis been accomplished?

For each maintenance level, has a decision been made for each item on how built-in test, automatic test equipment and general purpose electronic test equipment will support fault detection and isolation?

Is the planned degree of test automation consistent with the capabilities of the maintenance technician?

For each item, does the planned degree of testability design support the level of repair, test mix, and degree of automation decisions?

Are the test tolerances established for BIT consistent with those established for higher level maintenance test?

Test Data

Do state diagrams for sequential circuits identify invalid sequences and indeterminate outputs?

If a Computer-Aided Design system is used for design, does the CAD data base effectively support the test generation process and test evaluation process?

For Large Scale Integrated Circuits used in the design, are data available to accurately model the LSIC and generate high-confidence tests for it?

Test Data (cont'd)

For computer-assisted test generation, is the available software sufficient in terms of program capacity, fault modeling, component libraries, and post-processing of test response data?

Are testability features included by the system designer documented in the TRD in terms of purpose and rationale for the benefit of the test designer?

Is a mechanism available to coordinate configuration changes with test personnel in a timely manner?

Are test diagrams included for each major test? Is the diagram limited to a small number of sheets? Are inter-sheet connections clearly marked?

Is the tolerance band known for each signal on the item?

WT	Total Number	Number Meeting Criteria	Score	WT Score

10. SCOPE

10.1   Appendix C shall be considered as forming a part of the basic standard.

10.2   The purpose of this appendix is to provide definitions of terms used for clarity of understanding and completeness of information.   As a general rule, the definitions provided are currently accepted and have been extracted verbatim from other directives (regulations, manuals, MIL-STD's, DOD Directives, etc.).   A limited number of terms are presented for which definitions were developed from several reference documents.

20. DEFINITIONS

Acquisition phases

(a)   Concept Exploration Phase - The identification and exploration of alternative solutions or solution concepts to satisfy a validated need.

(b)   Demonstration and Validation Phase - The period when selected candidate solutions are refined through extensive study and analyses; hardware development, if appropriate; test; and evaluations.

(c)   Full-Scale Development Phase - The period when the system and the principal items necessary for its support are designed, fabricated, tested, and evaluated.

(d)   Production and Deployment Phase - The period from production approval until the last system is delivered and accepted.

Built-in test (BIT).   An integral capability of the mission system or equipment which provides an automated test capability to detect, diagnose or isolate failures.

Built-in test equipment (BITE).   Hardware which is identifiable as performing the built-in test function; a subset of BIT.

Cannot duplicate (CND).   A fault indicated by BIT or other monitoring circuitry which cannot be confirmed at the first level of maintenance.

Failure latency.   The elapsed time between fault occurrence and failure indication.

False alarm.   A fault indicated by BIT or other monitoring circuitry where no fault exists.

Fault coverage, fault detection.   The ratio of failures detected (by a test program or test procedure) to failure population, expressed as a percentage.

Fault isolation time.   The elapsed time between the detection and isolation of a fault; a component of repair time.

Fault resolution, fault isolation. The degree to which a test program or procedure can isolate a fault within an item; generally expressed as the percent of the cases for which the isolation procedure results in a given ambiguity group size.

Inherent testability. A testability measure which is dependent only upon hardware design and is independent of test stimulus and response data.

Interface device (ID). Provides mechanical and electrical connections and any signal conditioning required between the automatic test equipment (ATE) and the unit under test (UUT); also known as an interface test adapter or interface adapter unit.

Item. A generic term which may represent a system, subsystem, equipment, assembly, subassembly, etc., depending upon its designation in each task. Items may include configuration items and assemblies designated as Units Under Test.

Off-line testing. The testing of an item with the item removed from its normal operational environment.

Performing activity. That activity (government, contractor, subcontractor, or vendor) which is responsible for performance of testability tasks or subtasks as specified in a contract or other formal document of agreement.

Requiring authority. That activity (government, contractor, or subcontractor) which levies testability task or subtask performance requirements on another activity (performing activity) through a contract or other document of agreement.

Retest okay. A unit under test that malfunctions in a specific manner during operational testing, but performs that specific function satisfactorily at a higher level maintenance facility.

Testability. A design characteristic which allows the status (operable, inoperable, or degraded) of an item to be determined and the isolation of faults within the item to be performed in a timely manner.

Test effectiveness. Measures which include consideration of hardware design, BIT design, test equipment design, and test program set (TPS) design. Test effectiveness measures include, but are not limited to, fault coverage, fault resolution, fault detection time, fault isolation time, and false alarm rate.

Test program set (TPS). The combination of test program, interface device, test program instruction, and supplementary data required to initiate and execute a given test of a Unit Under Test.

Test requirements document. An item specification that contains the required performance characteristics of a UUT and specifies the test conditions, values (and allowable tolerances) of the stimuli, and associated responses needed to indicate a properly operating UUT.

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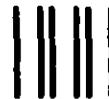
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