

EXPERIENCES GAINED USING THE NAVY'S IDSS WEAPON SYSTEM TESTABILITY ANALYZER

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ABSTRACT

The Weapon System Testability Analyzer (WSTA) being developed for the Navy's Integrated Diagnostic Support System (IDSS) program presents various features and capabilities to design engineers that can ensure a true "Design For Testability." A key feature of the IDSS WSTA is the ability to measure the testability of a design by modeling the actual process used during on-line, real-time fault diagnosis. This paper will present the results of experiences gained applying the WSTA to various levels of analysis, including: built-in test (BIT) assessment at the "0" or Organizational level; verification of complete testability from system, subsystem, and weapon replaceable assembly (or line replaceable unit) levels; and, through card level testability, detection and isolation accurately and efficiently at the piece-part level. The ease of modeling, the reports generated and their usefulness to the testability process, and the unique features associated with the use of the tool will each be discussed in the paper.

INTRODUCTION

Over the past several years, with the increased cost-consciousness on the part of Congress and the taxpayers, and with the resultant increase in the up-front investment required by military contractors, improved maintenance and support of both new and existing military systems have become priority concerns. In an era of mammoth leaps in the technology that is being designed into today's weapon systems, coupled with a decrease in the number of available military age personnel from which to draw, improved means must be developed to ensure that systems can be deployed and supported in the most economical and efficient manner possible. In 1985, the DOD released MIL-STD-2165, "Testability Program for Electronic Systems and Equipments."¹

On examining this standard, several key points are evident: first, testability addresses the extent to which a system or unit supports fault detection/isolation (FD/FI) in a "cost-effective manner." Given the complexity of today's weapon systems, it is not possible to accurately predict the overall testability of a weapon system without an automated tool to aid the design engineer. The second point evident in MIL-STD-2165 is that the "incorporation of adequate testability, including built-in test (BIT), requires early and systematic management attention." This re-emphasizes the need to develop and measure the overall testability of a system at all phases of its life cycle, from concept definition through deployment. This standard is an excellent program for managing a testability assessment program, and for documenting which parameters should be monitored to ensure that a system is testable.² However, an automated means of verifying compliance is essential for not only simplifying the process of performing a design for testability (DFT) analysis, but also as a means for reducing the up-front development costs associated with providing a testability analysis. The Integrated Diagnostic Support System (IDSS) contract, competitively awarded to Harris in 1986, provides such an institutionalized system of standards, guides, specifications, and tools to define, mandate, and support a structured process of maximizing diagnostic effectiveness.³ Of the IDSS system elements currently developed or being developed, the Weapon System Testability Analyzer (WSTA), is presently being used to provide testability guidance and analysis for several weapons and avionics platforms.

WSTA FEATURES

The WSTA is designed to interact with the designer - either the weapon system designer or test designer - to support the achievement of measurable DFT goals and to ensure the testability of the final design. In support of these goals, the WSTA provides the following functions:

Model Generation

Data Input. The WSTA will automatically, or with user assistance, generate a model representation of a unit under test (UUT). This model is based on dependency model theory and may be applied to any type of system, electrical, mechanical, hybrid, hydro-mechanical, or any combination thereof. The data to be used to generate this model can either be entered into the WSTA manually, or, in the more common case, extracted from a CAE/CAD system and stored in the IDSS Common Diagnostic Data Base (CDDDB). Current CAE/ CAD systems from which automatic data transfers have been accomplished are Daisy and Hewlett-Packard. Since entering the data for model generation has been proven to be a time-consuming operation with previous testability analyzers, the ability of the WSTA to perform this operation with minimal user interaction has proven to be a tremendous time (and thus cost) saver in the generation of testability models. In addition, many errors due to incorrect keying-in of model data have also been eliminated.

Once the model data has been entered, the next step is for the user to verify that the data entered is sufficient to provide an accurate representation of the testability performance of the UUT. In many cases, particularly with low density digital systems, the data extracted from the CAE/CAD system will not need to be modified prior to performing testability analysis. In certain other situations, the reverse is true. These differences occur due to the many ways that the testability of a system can be represented. The primary concern in performing a testability analysis, regardless of the tool being used, is to be able to accurately describe each failure mode of the system. Since digital circuits are generally considered to fail either stuck HI or stuck LO, the data from the CAE/CAD system is sufficient in these cases. For systems with multiple failure modes, the various faults must presently be represented manually. It is at this point where the second time-saving feature of the WSTA comes into play - the WSTA Model Editor.

Model Editor. The Model Editor provides the WSTA user the ability to create, augment and/or modify a model used to analyze the testability of the UUT.⁵ The Model Editor has been shown to provide many cost saving features not usually associated with an analysis tool of this nature.

The WSTA Model Editor allows the designer to manipulate six kinds of model elements, as shown in Figure 1: test points, components, tests, aspects, dependencies, and loops. A test point is defined as any physical location on a particular UUT that can be measured or observed to provide an indication of the health of the UUT. Examples of test points that have been included in models to date are: edge connector pins, BIT indicators, a node between two components that may be probed, a light that may be observed, a BIT software test that can be performed, as well as similar other cases. As more experience is gained about what constitutes a testable system, more information will be included in the testability analysis for future systems. Tests are the actual

measurements and/or observations that are conducted at the test points, and, together with aspects, form the heart of the WSTA's testability analysis power. Components are what they are normally thought of as, for example an IC, a resistor, a power supply, a pump. Components are those elements of the UUT that are the replaceable pieces of the system. An "aspect," on the other hand, is used to relate the various failure modes of a component to the appropriate dependency. Using these pieces as building blocks, it is now easy to see how the WSTA uses a dependency model: A dependency model consists of relationships between aspects and tests; an aspect, if faulty, "depends" on input tests to determine the state of its output. What the Model Editor provides to the user is an object-oriented editing/input capability; that is, if the user wishes to make a change to a test or component, the WSTA automatically collects all information about that model element (object) and presents it to the user in the form of windows. It becomes easily apparent to the user when a change will affect multiple model elements. This feature has proven to be extremely valuable, not only in correcting modeling errors or adding dependency relations, but also in helping to keep track of design changes that occur prior to production and that must be tracked to determine the overall impact on the testability of the system.

Also included as part of the WSTA's testability analysis tool box is the ability to include logistics data in its decision making. Traditionally, testability has been carried out, manually or otherwise until the advent of the WSTA, with no concern for how a UUT might be physically configured. Since in reality the proof of the testability of a piece of equipment is in how repairable it proves to be once deployed, logistics factors such as mean-time-to-replace, mean-time-between-failure, mean-time-to-isolate, etc., should be included in any testability analysis if meaningful results are expected. The WSTA uses these data in calculating an optimal test strategy for on-line fault diagnosis; this test strategy is in turn used by the WSTA to provide "dynamic" Testability Figures of Merit (TFOM) which give further insight into the overall testability of the UUT than is possible using only a structural analysis. The logistics data can be automatically extracted from a

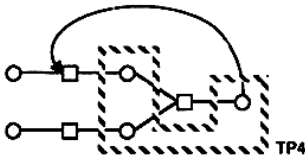
Logistic Support Analysis (LSA) data base, it can be manually entered into the CDDB by the user via the Model Editor, or default values can be used if data is not available. As is the case with circuit data, the highly sophisticated Model Editor allows the user to add or modify any logistics data element and aids the user by providing the relationships between tests and components and their associated logistics data. Not only does the WSTA provide meaningful TFOM by modeling the on-line process used during fault isolation, but the WSTA also provides an efficient, cost effective tool for monitoring and measuring these TFOM.

Testability Analysis

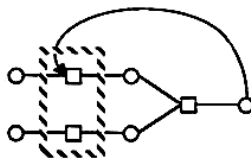
Once the UUT model has been successfully generated using the features mentioned above, the next step is to perform the testability assessment. For the WSTA, this function is performed using the function called, appropriately enough, the Testability Analyzer. This analyzer enables the user to perform two types of analysis. First, a "static" analysis, based solely on the interconnection of dependency elements can be directly derived from the netlist, or topology, of the UUT. The second type of analysis, unique to the WSTA, is what is referred to as "dynamic"; this analysis is modeled after the real world, on-line fault detection/isolation diagnosis process.

Static Analysis. In generating Static Testability Indicators, the WSTA uses the model created during the model generation process and computes the following TFOM:

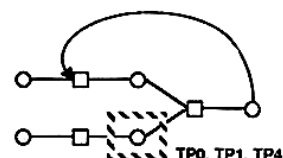
1. Inherent Fault Isolation Levels - This is the traditional "scoring" factor, commonly referred to as "isolation to x components y percent of the time, etc." This feature is rapidly calculated by the WSTA and has proven to be an excellent first-cut indication of the overall testability of the UUT.
2. Ambiguity Group Distribution - This is a tabulation of each of the ambiguity group sizes that will result from the current structure of the UUT.



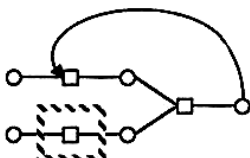
TESTPOINT IS A PHYSICAL LOCATION WHERE TESTS CAN BE PERFORMED. A TESTPOINT CAN BE ASSOCIATED WITH MANY TESTS.



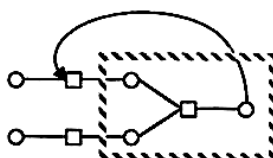
A COMPONENT IS A PHYSICAL PIECE OF HARDWARE. IT CAN HAVE MANY ASPECTS.



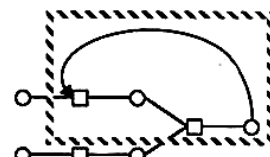
A TEST IS A NODE IN THE DEPENDENCY MODEL. IT CAN REQUIRE MANY TESTPOINTS TO PERFORM THE TEST.



AN ASPECT IS A NODE IN THE DEPENDENCY MODEL. IT CORRESPONDS TO A FAILURE STATE.



A DEPENDENCY IS A TEST, THE ASPECTS WHOSE OUTPUT IS THE TEST, AND THE INPUT TESTS TO THOSE ASPECTS.



A LOOP IS A LIST OF DEPENDENCIES WHERE A SIGNAL FEEDS BACK ON ITSELF.

Figure 1. Model Elements

3. Component Involvement Ratios - This is a measure of the relative frequency with which each component will appear in any ambiguity group. This is valuable information, since components that appear frequently must be made either highly reliable or readily accessible for repair, or both.
4. Controllability/Observability - Paramount in importance in being able to generate tests that will take full advantage of the testability of a system is the ability to "control" a component so that its output may be "observed." This information is derived from the WSTA model for each component, input pin, output pin, and test point, and provided to the user for analysis of the ease or difficulty of performing the required tests.
5. Feedback Loop Report - A typical cause of large ambiguity groups is feedback loops. While it is recognized that many loops may not be broken, for functional reasons, it is also recognized that there are in many system feedback loops that may, upon careful analysis, be eliminated or modified such that large ambiguity groups can be reduced to acceptable levels.
4. Test Point Utilization Data - a measure of how often each test point appears in a given test strategy. This information is also used by the DFT Advisor when making recommendations for improving the overall testability of the UUT by changing test points.
5. Test Point Criticality - A measure of the aggregate criticality of the components associated with a given node in the test strategy, this data is provided to determine those components that should be made more reliable and/or more accessible due to their inherent criticality to satisfactory performance of the UUT.

Of the two forms of testability analysis available to the user, current experience has shown both to be very valuable for different reasons. Static analysis has proven invaluable in calculating data required for completion of the Appendix B checklist of MIL-STD-2165, while dynamic analysis provides insight into what the actual testability of an UUT can be, and, coupled with the DFT Advisor, has been an excellent aid in adding/modifying test points. In addition, the ability to generate, almost effortlessly, a diagnostic test strategy that can either be used by an on-line monitoring program such as the ADS, or used directly as a replacement for the diagnostic flow chart generated as part of a test program set, makes the WSTA an extremely time/cost saving tool.

Dynamic Analysis. To determine the testability of the UUT based on real world conditions, the WSTA calculates a "strategy" which provides an optimal or near optimal sequence of diagnostic tests for isolating each and every component in a given model. The resultant test strategy may, and has been, utilized directly by a test program set (TPS) designer, or any on-line tool such as the IDSS Adaptive Diagnostic System.⁶ The test strategy generated by the WSTA is based on an enhanced version of the TEST (Time Efficient Sequencer of Tests) algorithm.⁷ This algorithm employs a top-down search (i.e., forward chaining with backtracking) method that integrates concepts from information theory and artificial intelligence to reduce the computational explosion that would otherwise occur during the construction of an optimal diagnostic fault tree. For the current version of the WSTA, two modes of Test Strategy Generation are employed: mode one, single step look-ahead, computationally less intense than mode two, but useful as a quick check on the overall testability of the UUT; and mode two, multi-step look-ahead, which includes a user-selectable degree of desired optimality. Mode two may be applied iteratively until the desired degree of optimality has been achieved.

Design for Testability Advisor

Once the testability of the UUT has been assessed, the user is presented with at least two options to follow: the first, and ideal case, is that the UUT meets each and every one of the testability requirements that have been imposed on it. In this ideal case, no further analysis is required, and the job of the user is complete. In the more common case, however, the user is presented with quite a different situation: the UUT has failed to meet its testability requirements, and the user is responsible for making changes or recommendations for improving the UUT's testability performance. It is in this case that previous testability analyzers have fallen short; the testability of a UUT will be reported via some sort of report (with the testability analyzed only from a static standpoint), and the user is left on his own to figure out how to improve the testability of the UUT. In the case of the WSTA, the Design for Testability (DFT) Advisor analyzes the static and dynamic testability indicators and provides the user with a comprehensive set of recommendations for improving the testability of the UUT. The major recommendations provided are the following:

Once the test strategy has been generated, the WSTA provides to the user dynamic TFOM. The term dynamic is used in a dual sense: the first, to distinguish this analysis from the topological, or static analysis; and, second, to emphasize the fact that the TFOM represent the testability performance that can be expected to result during an actual, on-line fault diagnosis session. Using this dynamic strategy, the following TFOM are provided:

1. Isolation penalties - mean-time-to-isolate (MTTI) and mean-cost-to-isolate any faulty component in the UUT.
2. Repair Penalties - mean-time-to-repair (MTTR), based on individual isolation times obtained automatically from the logistics data stored in the CDDB, coupled with individual component replacement times, and, similarly, mean-cost-to-repair.
3. Replacement/Isolation Tradeoff Data - This data is provided to the user to provide visibility into the overall testing picture for the UUT: sometimes, it may be cheaper to stop testing with a somewhat larger than ideal ambiguity group than to incur the increased expense of additional testing, and this data will help the user make that determination.
1. Loop-Breaking Recommendations - The optimal point to break each feedback loop, including a hierarchical list of alternatives, is provided for each feedback loop in the model. This feature has proven to provide insight into solving complex feedback loop problems in much less time than would be required if a manual analysis were to be performed.
2. Test Point Recommendations - Based on an analysis of the static and dynamic testability indicators, the WSTA provides three types of test point recommendations not found in any other testability analyzer on the market today:
 - a. BIT Test Point Recommendations - Based on test strategy developed by the Dynamic Testability Analyzer, the WSTA will select the minimum set of test points required to certify a UUT as being good.
 - b. Test Points to Delete - Based on a combination of redundant tests from the Dynamic Test Tree, coupled with the static analysis from the dependency model, the WSTA provides a list of all test points that can be

deleted with no effect on the overall testability of the UUT. This information is crucial for cases where the testability falls short of its requirements, and all connector pins have been allocated. By selecting from this list, the user can make room for pins that will provide meaningful information.

- c. Test Points to Add - Using information provided by the user concerning which nodes in the UUT should be considered as test points, and which ones have not been selected, the WSTA provides a list of those nodes that will, if made into test points, improve the overall testability of the UUT. This information is based on calculations made by the WSTA, where each of these nodes is temporarily considered a test point, and the resultant percentage improvement in MTTR is calculated. Those test points that show the highest improvement are listed as the most likely candidates for adding to the UUT. This data would be extremely difficult and time-consuming to calculate manually, and is a definite improvement over the usual means of adding test points to improve testability, namely guessing.

CONCLUSION

As shown above, the IDSS WSTA has already proven to be a valuable aid to measuring and monitoring the testability of various UUT's. The ease of data entry, primarily the ability to extract model data directly from a CAE/CAD system, provides to the user a tool with capabilities not found in any other testability analyzer. The WSTA, by providing various means of performing testability analysis, allows the user to reap benefits for the overall supportability of the UUT that transcend typical MIL-STD-2165 analysis. The WSTA provides the user information on not only what the results of the testability analysis are, but also provides guidance as to how to design the most testable UUT possible. Thus, the WSTA has proven to be the answer to the question of how to provide an automated, cost-effective means of verifying

that today's systems can be deployed and supported in the most economical and efficient way possible.

ACKNOWLEDGEMENT

This work was partially funded by NAVSEA contract N00024-87-C-4033.

I am grateful to James M. Scott, Harris Corp., for assistance in the preparation of this paper.

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