Prime equipment hardware structures which support the test process. This includes partitioning, test access and test control. The modules of the prime equipment should be designed such that the ATE system has sufficient control of the unit under test and sufficient visibility of the unit's internal operation to allow quick, comprehensive and low-cost testing.

Testability Measures

If testability is to be specified as a requirement, there must be ways available to measure the degree of testability implemented in a system. There are three different kinds of testability measures which may be applied to a system, depending upon its stage of development. The three may be called Inherent Testability Prediction, Comprehensive Testability Prediction, and In-Service Testability Measurement. The use of these measures is depicted in Figure 1. The first two measures are based upon models of hardware and actual failures. This points out the importance of specifying a realistic failure universe (failure model) to serve as the basis of early testability design and evaluation.

Inherent Testability Prediction.

These measures are applied during preliminary design, prior to development of any test stimulus/response data, to predict how well the prime equipment will support the test process. Some inherent measures include ATE compatibility checklists and the degree of observability and controllability of internal circuitry by the test system (BIT or ATE).

Comprehensive Testability Prediction

These measures predict the ease, speed, economy, and the confidence with which testing may be achieved. Important testability parameters include fault coverage, fault detection time, fault resolution, and fault isolation time.

Testability Effectiveness Measurement

This set of measures gives an indication of how well the design is supporting the test process in the actual system environment. Measures at this point are similar to maintainability measures and include fault isolation times using BIT and ATE, and false alarm rates.

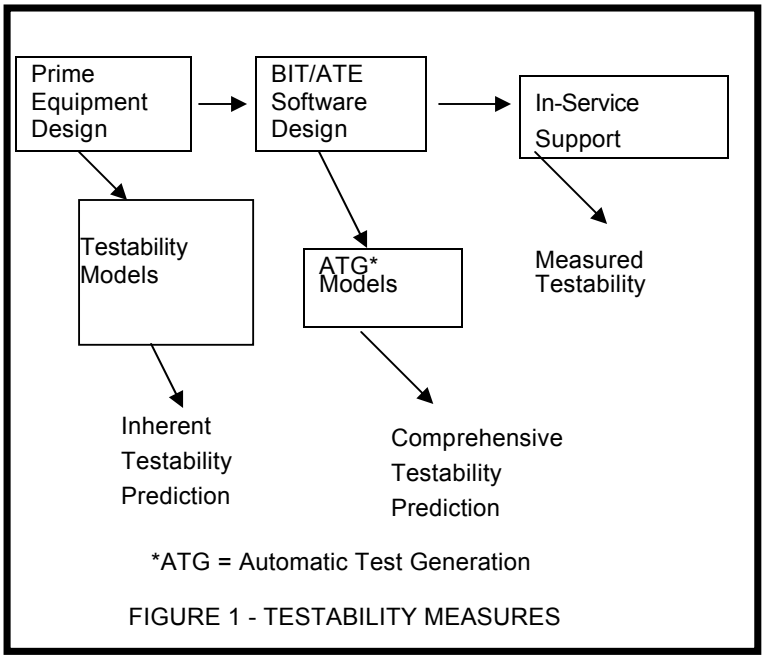

FIGURE 1 - TESTABILITY MEASURES

Achieving Testable Systems

Design for Testability is not yet a universally accepted practice within DoD, although the JLC Testability Program is providing much needed visibility for DFT throughout the Services. Design for Testability can become an accepted practice within DoD only if three things happen:

1. Necessary technology is available,
2. Management incentives exist to incorporate testability, and
3. Meaningful testability standards are available.

Technology

BIT techniques have been successfully applied to many diverse systems and many testability design guides exist within industry. Given that changing technologies will demand continuing development of DFT techniques, much of what is needed for testable designs is well understood today.

Incentives

The need for management incentives to include testability applies to both DoD management and industry management. Official DoD policies support increased system readiness, minimized life cycle costs, and upfront consideration of logistic support requirements. In practice, program managers are under constant pressure to "make it work" and to defer support considerations until later, at which time DFT is, by definition, impossible.

Standards

Industry has successfully employed DFT techniques in commercial systems to reduce factory checkout, installation, and field service costs even though the DFT costs/ benefits analysis is often not formalized. In dealing with the government on a multi-phased, multi-year development, the up-front DFT costs are extremely visible and subject to close scrutiny and formal justification. Progress toward a testable design must be measurable at each major review point and related back to requirements.

The Industry/Joint Services Automatic Test Project (I/JSATP) recognized that many problems in achieving testability are managerial in nature and concluded that DoD and the Services must impose verifiable testability requirements during the design process and enforce compliance if testability is to become a major factor (Ref. 4). The 1980 JLC DFT subtasks are consistent with the recommendations of the industry project and address the development of policies and procedures for managing testability, the development of testability design guides, and the development of military standards and specifications for testability.

Navy DFT Program

The four JLC testability subtasks in Table 1 for which the Naval Material Command has primary responsibility are:

1. Joint Service Built-in Test Guide
2. Testability Program Review
3. Fault Tolerant Design
4. Testability Figures of Merit.

Joint Service BIT Guide

This guide was developed by the Naval Ocean Systems Center (NOSC), San Diego in 1980 and is available to government and industry personnel. The guide presents the fundamentals of built-in-test, provides an overview of different BIT approaches, and discusses BIT evaluation techniques. The guide includes specific examples of built-in-test which have been applied to military radar, communications, signal processing, and computer systems. The guide is intended for use by design engineers who are responsible for translating BIT requirements into equipment designs in an optimum manner considering equipment reliability and maintainability requirements.

Testability Program Review

The Test and Monitoring Systems Program Office within the Naval Material Command (MAT 04T) has completed a review of documents and processes used to conduct weapon system program reviews and is formulating updates to reflect increased emphasis on testability issues. As a result, testability and other supportability issues will receive earlier and increased attention at weapon system reviews.

Fault Tolerant Design.

In certain applications, the incorporation of fault tolerant techniques is the only way to meet stringent reliability and readiness requirements. This Navy (NOSC) subtask will develop methods for specifying and validating the performance of fault tolerant computers embedded in weapons systems.

Testability Figures of Merit

This subtask, performed by the Naval Surface Weapons Center (NSWC), Dahlgren, Virginia is developing figures of merit such that testability parameters may be quantitatively specified, demonstrated, and evaluated. This effort includes the development of a Military Standard on Testability Requirements which integrates the various figures of merit into a standard framework for testable design (Ref, 5).

Summary (Navy)

Most project managers, in government and industry, are aware that testing costs may be significantly reduced by the early consideration of testability (including built-in-test and fault tolerance) in prime equipment design. In addition, techniques for such designs are generally well understood by industry and have been successfully incorporated into several products. The item that is missing in acquiring testable systems and equipments for DoD is a general framework for determining requirements, trading off alternatives, measuring progress and demonstrating compliance. The Navy efforts promote a unified approach to dealing with testability during all phases of equipment development.

The Air Force Testability Program

The chief Air Force Agencies developing design tools for Testability are the Air Force Wright Aeronautical Laboratories (AFWAL), the Modular Automatic Test Equipment (MATE) project office, and the Rome Air Development Center (RADC).

In 1978, AFWAL began a five year study to develop guidelines for the Ease of Maintenance of Avionic equipment. Results of the first year study phase are available in a report, AFAL-TR-79-1130 "Design for Repair Concept Definition." The MATE office, located in the Ads Force Systems Commands' Aeronautical Systems Division, is responsible for developing an Air Force approach to cost-effective Automatic Test Equipment, which includes development of testability concepts. Results of this program will include testability design guides as well as a recommended modular ATE design concept. To maintain independence between the two competing MATE contractors, no reports have been released thus far.

The most significant Air Force Testability program, in terms of published information, has been the RADC program.

The RADC Testability Program

The Rome Air Development Center (RADC) is charged with the development of techniques for Predicting, Demonstrating and Improving Reliability and Maintainability in Electronic Systems. In 1977 the Center was in the midst of a program to modernize the maintainability engineering discipline and discovered the greatest needs in maintainability engineering were techniques for the specification, design and measurement of fault detection and isolation parameters. These techniques can be considered a subset of maintainability techniques, but are important enough in their own right to deserve the specific title of Testability Engineering Techniques. Thus, the RADC Testability Program was born.

At this time, RADC considered testability a greatly neglected engineering discipline with a significant impact on Life Cycle Costs. As an illustration, RADC was tasked by the Air Force Systems Command to study the feasibility of creating a family of specifications for digital printed circuit board (PCB) testers to cover Air Force needs. The idea was to provide government furnished testers in lieu of expensive custom built units. A survey was made of existing and potential Air Force applications and of the capabilities of commercially available digital PCB testers. It was concluded that the vast majority of Air Force applications could be met with available testers. Hence, neither custom built units nor an Air Force family of testers was required. An immediate application of the study was made by the Air Force 427M Program Office, who rejected a proposed custom built digital printed circuit board tester with a price tag of four million dollars in favor of a commercially available tester costing one million. This example clearly illustrates that there are significant savings to be made by careful attention to testability. In addition, it shows the lack, at the time, of an organized testability engineering discipline. RADC, therefore, embarked on a program with the deliberate intent to create a test-ability engineering discipline.

Figure 2 shows the events since that decision. While work progressed on developing the fundamentals of an engineering discipline, an attempt was made to provide some useful products immediately. These interim products were created by a review and distillation of existing information from a variety of sources. These included RADC maintainability studies, a study of built-in-test effectiveness by the Air Force Aeronautical Systems Division, several Navy publications, the work of the Automatic Test Equipment Committee and a surprising amount of information from the Industry Internal Research and Development Program. In fiscal year 1979, these interim products were released. In fiscal year 1980, six RADC studies were published which the Center believes provides the essential foundations of the Testability Engineering Discipline. Future work will refire and mature the discipline, with RADC efforts closely coordinated with many other agencies. Besides those mentioned above, the Air Force Modular Automatic Test Equipment Office, the Air Force Acquisition

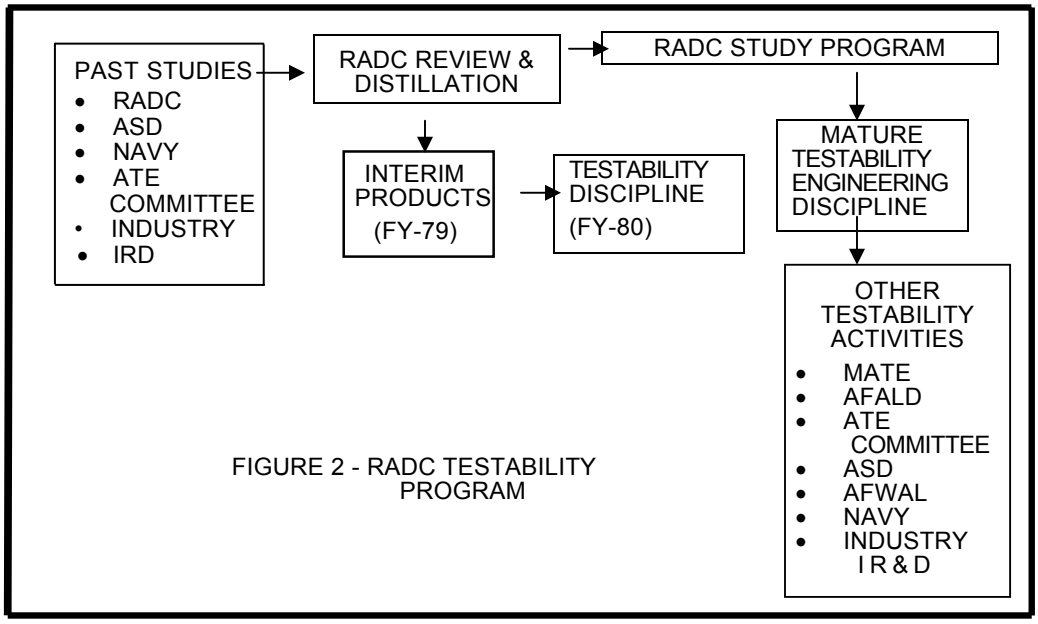

FIGURE 2 - RADC TESTABILITY PROGRAM

Logistics Division and the Air Force Wright Aeronautical Laboratories have a significant interest in testability and will contribute to the mature discipline.

Figure 2 presents the overall RADC program. The remainder of this paper will describe the interim products, the foundations of the Testability discipline, and the current RADC Testability Program.

The interim RADC products were designed primarily to provide the Air Force Electronics System Division - (ESD) with useful techniques while the discipline was being created. Accordingly, all of the information available to RADC was distilled into an ESD program office acquisition guide. This guide attempted to integrate testability considerations into the normal Air Force program development cycle, rather than establish additional program management procedures. A draft of this report was provided to the Air Force Acquisition Logistics Division (AFALD), who condensed it into a testability checklist which they provided to all AFALD personnel assigned to System Program Offices as Deputy Program Managers for Logistics.

The most glaring need in testability in 1979 was for a procedure for measuring the performance of system fault detection and isolation features. The RADC interim guidelines provided a workable procedure documented in MIL-STD-471A, Notice 1 (USAF) an Air Force addition to MIL-STD-471A "Maintainability Demonstration." A revision of MIL-STD-471 is being prepared by RADC which will incorporate Testability demonstration features into the fully coordinated standard.

In 1977, RADC had prepared MIL-STD-1591 "On-Aircraft, Fault Diagnosis, Sub-Systems, Analysis/ Synthesis of" providing a mathematical procedure for optimizing on aircraft test systems. The interim guidelines included a generalization of the method applicable to ESDs ground systems, documented as MILSTD-001591A (USAF) to be used by the Air Force in lieu of MIL-STD-1591.

To aid the designers, RADC-TR-78-224 "A Design Guide for Built-in-Test" was published. This guide and several Navy documents are being combined by the ATE Committee into a proposed Tri-Service guide.

The final interim product was a computer program to aid in the selection of digital printed circuit board testers. This program was a key part of the digital printed circuit board tester study mentioned above, and matches the board test needs to the tester capabilities. After the study was completed, the program was loaded into the RADC computer. RADC then offered to run the program for any Air Force program manager who wished to use it as an aid to test equipment selection. The offer was accepted by several ESD program offices. One office, TRI-TAC, was using an interface board which they feared might require an EQUATE system, at $800,000, as a tester. The RADC program found a $15,000 tester which would do the job. The program has since been expanded to cover analog PCB testers and the service is still available at RADC.

While the interim products were being produced, work went on to complete the foundations for a testability engineering discipline. These started with the premise that a working engineering discipline needs specifiable figures of merit, demonstration procedures, design tools and cost trade-off procedures. Each of these needs was addressed by one or more RADC studies whose results were published in fiscal year 1980. The first report available was "BIT/External Test Figures of Merit and Demonstration Techniques," RADC-TR-79-309. As the title indicates, it addresses the first two needs cited above. The report examines 18 different measures of test equipment performance and provides for each a recommended means of demonstration.

Design Tools were addressed by three RADC studies. "Design Guidelines and Optimization Procedures for Test Subsystem Design," RADC-TR-80-111, provides straight-forward mathematical tools, algorithms and trade-off procedures useful to the designer for optimizing test subsystems to meet specified requirements. "An Objective Printed Circuit Board Testability Design Guide and Rating System," RADC-TR-79-327, attacks the problem from the other end. It provides a means for evaluating the design of a printed circuit board for ease of testing, thus permitting the creation of more testable boards, reducing test re-requirements. "Built-In-Test and External Tester Reliability Characteristics," RADC-TR-8O-32, presents the results of a study of tester impact on the reliability and down time of the prime system, a design concern especially significant for systems using built-in-test.

Cost-Tradeoffs are a prime concern of the program - manager. Testability cost trades are the subject of two RADC reports. "Operation and Support Cost of Characteristics of Testers and Test Subsystems," RADCTR-79-334, provides information on the cost of supporting the test system, a significant factor in system Life cycle costs, and a relatively neglected factor. "Availability/Operational Readiness-Test Subsystem Cost Trade-offs," RADC-TR-80-182, provides guidance in developing cost-effective tester requirements from basic system requirements such as availability.

The results of the preceding studies are all avail-able. Now in progress by RADC is the development of a testability notebook to consolidate this information and other developments into a single source for the program managers and system designers. Also in progress are studies on the causes of unnecessary removals and false alarms. About 301 of all avionic maintenance actions result in no failures found. An understanding of the causes for this may help significantly reduce this fruitless expense. Too frequent false alarms have in at least one instance negated the usefulness of an aircraft trouble recorder. It is also a serious problem in non-military applications such as nuclear power plant control rooms. Hence, the RADC study could have an extremely high pay-off.

In the future, RADC studies will cover analytical procedures for Testability, adapting the tools of Operations Research to the testability problem. Fault tolerance design procedures for distributed systems, considering both hardware and software, will be developed. Cost studies will include built-in-test hardware vs. software trade-offs and tester software cost estimation. Procedures for condition monitoring of non-electronic devices used in electronic systems, such as engine generators, will be developed and design guide-lines for programmable interfaces will be formulated.

Summary (Air Force)

Testability studies continue to promise a high pay-off. So long as tools are needed for the creation of cost-effective fault detection and isolation features in electronic systems, the Air Force Testability Programs will continue.

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Bill Keiner is an engineer in the Electronics Systems Department at the Naval Surface Weapons Center. He was involved for several years in the development of maintenance procedures and software for the Navy's Polaris and Poseidon missile fire control computers. Later, he directed the development of state-of-the-art logic simulation tools for fault analysis of the Trident computer designs. Bill has been actively involved in Navy-wide test technology matters since 1977 with an emphasis on defining a framework within which test-ability design parameters may be specified and evaluated for new Navy systems. Part of this Design for Testability (DFT) framework involves the development of quantitative figures of merit for assessing the testability of a design. Bill has served as Service Advisor to the Industry/Joint Service Automatic Test Project on DFT matters and has coordinated the JLC testability subtasks. He has also developed material on DFT techniques which was incorporated into a Joint Service DFT Course.

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Mr. Anthony Coppola was born in Brooklyn, New York on July 14, 1935. He holds a Bachelor's Degree in Physics and a Master's Degree in Engineering Administration, both from Syracuse University. He is Chief of the Reliability and Maintainability Engineering Techniques Section, Rome Air Development Center, and is responsible for developing methods for predicting, demonstrating, and improving the Reliability and Maintainability of Air Force electronic systems. He has been a member of the faculty of the Air Force Institute of Technology School of Systems and Logistics and of the staff of the George Washington University School of Engineering and Applied Science. He is a Senior Member of IEEE, past Chairman of the Mohawk Valley Section, and the organizer and first Chairman of the Mohawk Valley Chapter of the IEEE Reliability Society.