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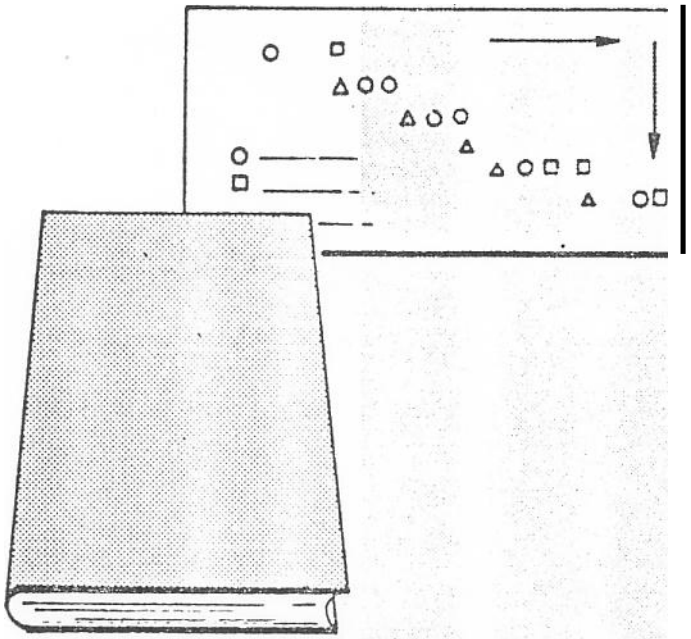

DESIGN DISCLOSURE FORMAT DEVELOPMENT

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DESIGN DISCLOSURE FORMAT DEVELOPMENT

In this talk, I will identify and describe the four basic forms of design disclosure formats: the blocked schematic diagram, the precise access block diagram, the blocked text, and the design outline. In discussing one type of design outline, the maintainability disclosure chart, I will point out how critical maintainability data can be derived for the system under design. The synthesis of such data constitutes an objective maintainability prediction for system evaluation by project management. The analysis of such data can reveal areas for additional maintainability design or modification efforts.

As we all know, the maintenance that is performed on an equipment or system is really a measure of the maintainability that was built into a system during its design phase. I shall ask you to keep two thoughts in mind during this talk. The first is that maintenance is considered to be an action performed after the fact, while maintainability design is the action performed during the fact, or, while an equipment or system is being designed. The two should be compatible. If they are not, we, as managers, have initiated a problem which will remain with us for quite a while. Let's begin our explanation of how we can avert such problems by examining the design disclosures and what they can provide for us. I have chosen this to begin our talk so that we may begin our exploration into the design disclosure formats with a common basis from which to judge them throughout the remainder of the discussion.

1. QUICK REACTION TO PROBLEM AREAS
2. COMPREHENSIVE EVALUATION OF CONTRACTOR PERFORMANCE
3. THOROUGH ANALYSIS OF ANY SYSTEM OR EQUIPMENT UNDER DEVELOPMENT
4. UNAMBIGUOUS DIRECTION OF THE TOTAL DESIGN BY YOU PROJECT MANAGERS
5. LASTLY, A CONSTANT SURVEILLANCE OF PROGRESS

I'm sure you will admit that each point is important and is constantly in the mind of each program manager. I am likewise very certain that if each of these goals could honestly have been said to be accomplished, they would enable a program manager to actively participate and provide positive direction to contractors throughout the entire life cycle of the equipment or system. But, how certain are we that we have really accomplished all of these high-sounding objectives? Do we really have the tools to make these decisions? This leads us to an explanation of the basic techniques of the design disclosure formats and how they will help us fulfill our obligations as true program directors.

There are four basic structures in the design disclosure formats. These are the blocked schematic diagram, the precise access block diagram, the blocked text, and design outlines.

The blocked schematic diagram as shown in figure 1 serves the dual purpose of the unit schematic diagram and the unit functional diagram. It represents the most detailed level of design disclosure. The blocked schematic gives the same information as a conventional schematic, adds to it a precise definition of the components within a stage, and circuits within assemblies. and presents the information in its most understandable form. Circuits are drawn as the designer had conceived the design. No rearrangement of circuits are permitted by so-called present day drafting room manuals. During pertinent portions of an equipment's development in a life cycle we can detect what is equipment oriented, (that is, hard-

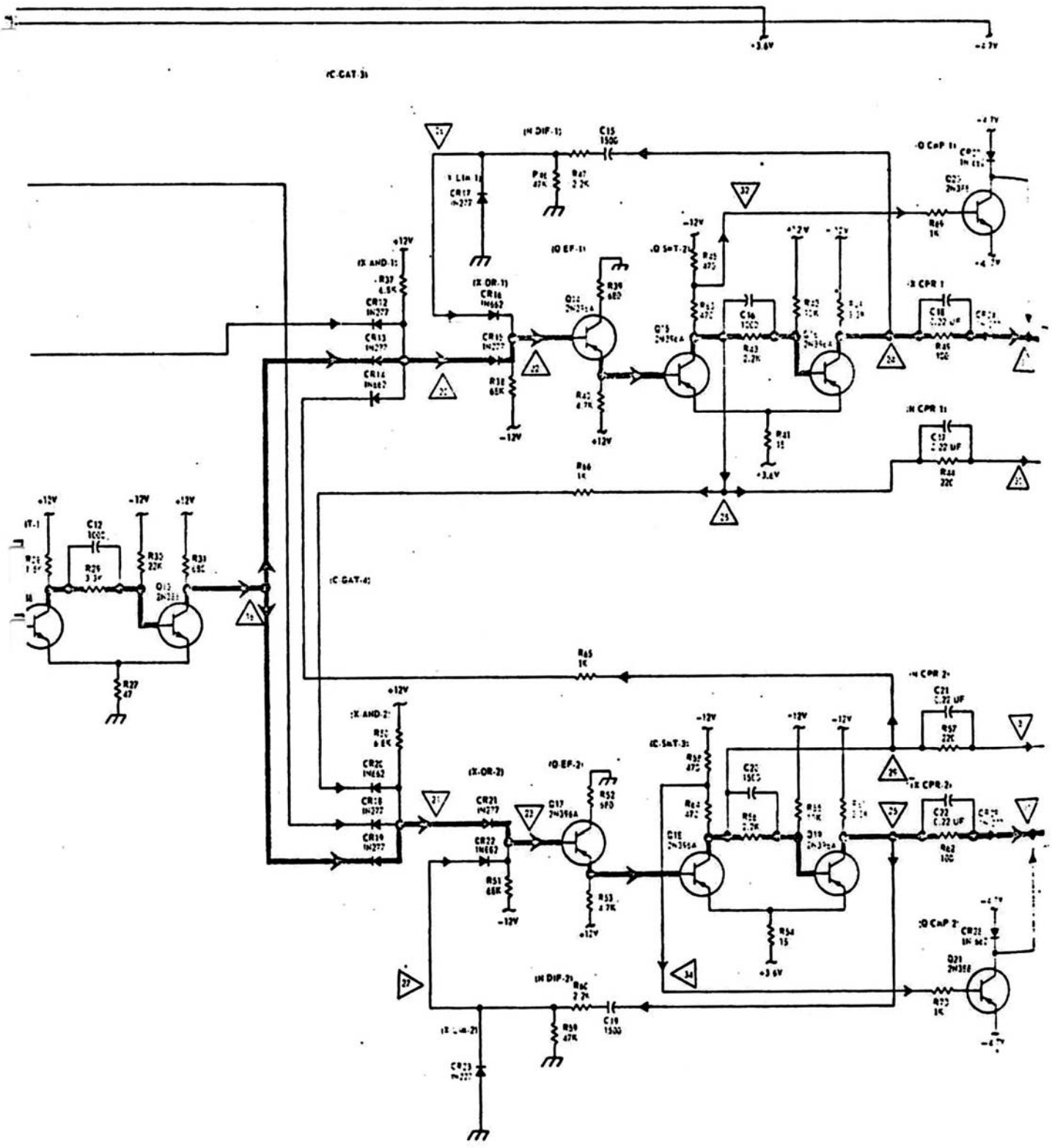


Figure 1.

ware oriented) or functionally oriented. The DDFs makes it possible to distinguish two things at all times, hardware and function. The blocked schematic uses shades of blue to group components within a stage and to define the functional boundary of each circuit within the assembly. Therefore, the blocked schematic takes the place of the conventional functional block diagram. Power and power filtering circuits are separated from the functional circuits, further clarifying functional operation of the circuit. The blue functionalization of circuits can be accomplished in the very early development stages or in any subsequent phase of the life cycle.

A light shade of grey over the entire area represents the hardware composition of the assembly. A removable subassembly is represented by a darker shade of grey. Many times we may not be able to distinguish between the separate levels of grey in the early development stages since we have not arrived at a packaging scheme. However, the functionalization should be understood and known to the program manager.

As a review of these different shades, we may say that the major blue shaded areas (the lightest blue shade) represents the major circuits within the assembly. The next darker blue shades define the lower order stages, or sub stage groupings, within a major circuit. The use of grey and blue shaded areas eliminates the confusing lines on blocks and hardware division, while giving the desired impression of increased levels of functional subdivision and hardware subdivision. Every component is there-fore identified as part of a particular functional circuit as well as part of an assembly or subassembly.

One of the innovations presented on the blocked schematic is the use of an alphanumeric code. This alphanumeric code is given in the top of each shaded area. The code is used as a precise means of identifying these same circuits on the related precise access block diagram, its associated hocked text, and on the design outlines. The alphanumeric code generally consists of four alpha units and a number. The first alpha unit identities the basic category of the circuit. If the major component of the circuit is nonlinear, it might be designated by V for vacuum tube, Q for transistor, or X for crystal diode. If the circuit contains several linear components, such as resistors or capacitors, it is designated as a network by the letter N. A composite, which contains two or more subordinate circuits, is designated by the letter C.

Clear functional flow is aided by a signal coding system. Each type of signal carries a unique form of arrowhead to define its function. Figure 2 illustrates some examples.

Compare the blocked schematic with the conventional schematic diagram (figures 3 and 4). The conventional schematic diagram has been prepared through normal channels present in most companies today. A designer's sketch was given to a draftsman who, using rules set forward in most drafting room manuals, provided a very balanced drawing, but one on which the circuits are hardly recognizable. The redrawn blocked schematic diagram more clearly depicts what the engineer probably had in mind, than the conventional schematic diagram with its undue clutter of lines, I am sure you can see which would be easier to review by both customer and contractor program managers. The next question to be asked is, "if the blocked schematic represents the basic engineering design as conceived by the engineer, why not make it compulsory that the drawing always be represented in this form?" Using design disclosure format rules the schematic will always be drawn as it has been conceived. Consequently, the blocked schematic diagram becomes easy to understand and also feeds back to stimulate the inventiveness of the designer.

PRECISE ACCESS BLOCK DIAGRAM

The precise access block diagram is the basis for much of the detailed design out-lines which we shall see later. By its very nature a conventional functional block diagram is not simple to explore or understand.

CODED ARROWHEADS AND EXPLANATION.

CATEGORY	SPECIAL SYMBOLS		
	BASIC SYMBOLS	FAULT SYMBOLS	
SIGNAL CODE SYMBOLS			MAJOR FUNCTIONAL FLOW, NORMAL
			SECONDARY FUNCTIONAL FLOW
			REFERENCE SIGNAL VOLTAGE
			FEEDBACK SIGNAL PATH
			SIGNAL PATH TO ENERGIZE RELAY
			GATING OR SYNCHRONIZING SIGNAL, OR LOWER LEVEL MODULATING SIGNAL METER READING
			TEST SIGNAL OR SIGNAL USED TO LIGHT LAMP OR PROVIDE
			TRANSMITTER PULSE-FORMING NETWORK DISCHARGE PATH AND SUBSEQUENT HIGH-LEVEL MODULATION PULSE
	MODIFICATIONS OF BASIC SYMBOLS		
			EMERGENCY SHORT PATH FOR POWER DISTRIBUTION
			BATTLE SHORT PATH FOR ENERGIZING A RELAY
			EMERGENCY SHORT PATH FOR ENERGIZING A RELAY

Figure 2.

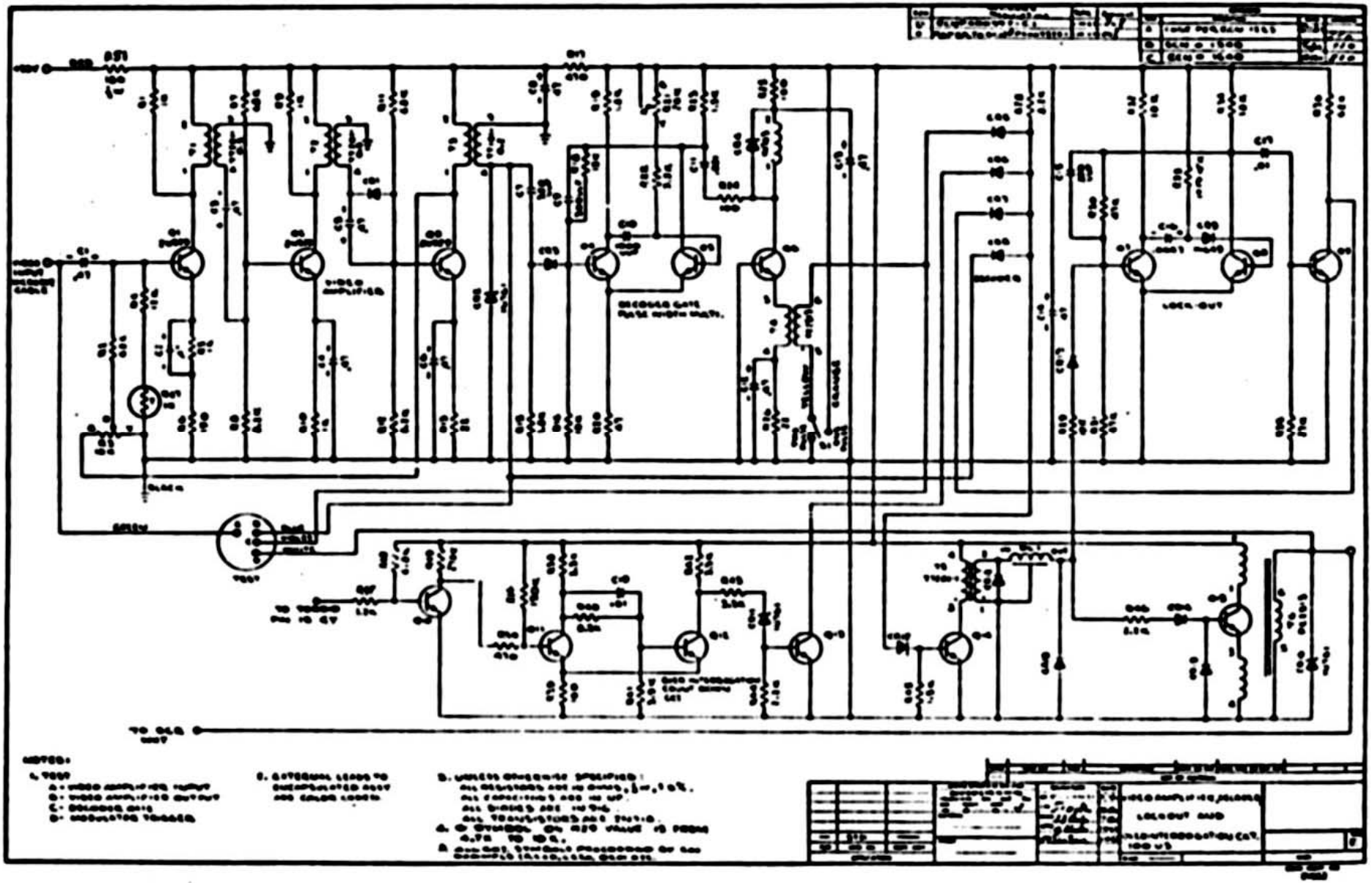
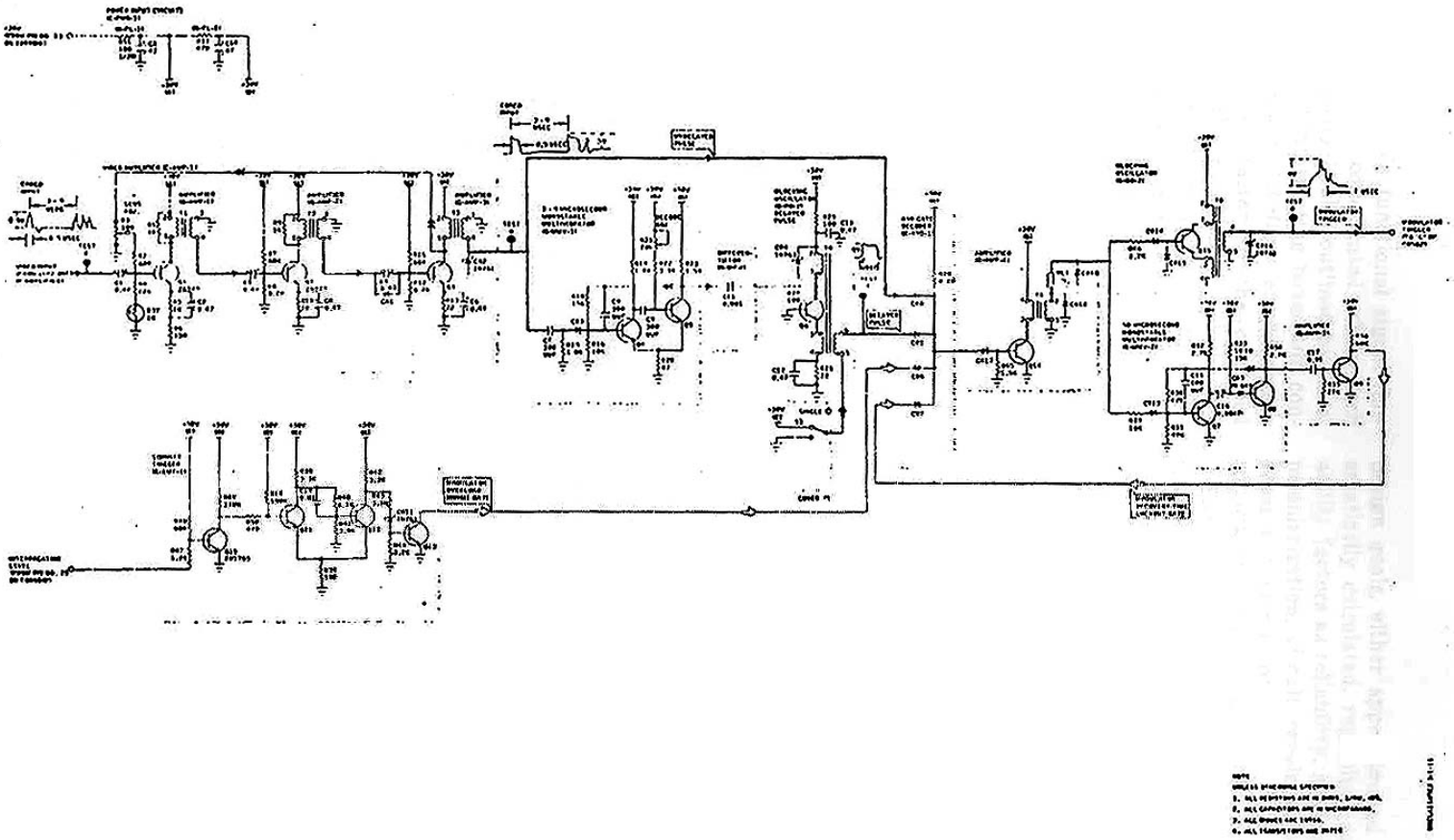


Figure 3.



VIDEO AMPLIFIER, DECODER, LOCKOUT, AND OVERINTERROGATION CIRCUIT — SCHEMATIC

Figure 4.

The relatively simple functional signal flow lines soon become complicated when each hardware boundary is also outlined by lines. Overlapping and intersecting boxes add confusion. Haphazard labeling of hardware blocks is another factor in the confused picture. With the conventional block diagram and schematic diagram as tools, designers as well as program managers, often find in extremely difficult to locate circuits within the system hardware. It is even more difficult to determine which components make up the circuit represented by the block in the block diagram.

Now look at a part of the precise access block diagram on which the system function of a driver amplifier is diagramed. (See figure 5.) The simplicity of the functional flow is uninterrupted when shaded areas are substituted for line hardware boundaries. Remember, on the blocked schematic, the grey shading defines hardware boundaries.) On the precise access block diagram, the meaning of the shading becomes apparent. The lightest shade of grey indicates the highest level of hardware, the cabinet.

The next darker grey shade represents the drawer or unit. The third level is the assembly. and the fourth level is the subassembly. The grey shading gives a psychological illusion of depth as we go deeper into the physical packaging of the equipment. Similarly, the blue shading gives a psychological illusion of depth as we go deeper into the functional grouping of the circuits. The shading technique provides a variable focus which allows the scanning of the big picture, and access to any detail that one may need. By modifying the configuration of the grey area, the left to right path of the signal flow can be maintained to a greater degree than ever before. To permit precise access to the blocked schematic diagrams each piece of hardware is identified by proper nomenclature in the top left corner of the shaded area.

The locked text, when presented for design disclosure purposes, may also include design goals, either approximated or mathematically calculated, regarding such avail-ability factors as reliability, maintainability, modularization, circuit repair times, sensor types and placement.

BLOCKED TEXT FOR SCHEMATICS

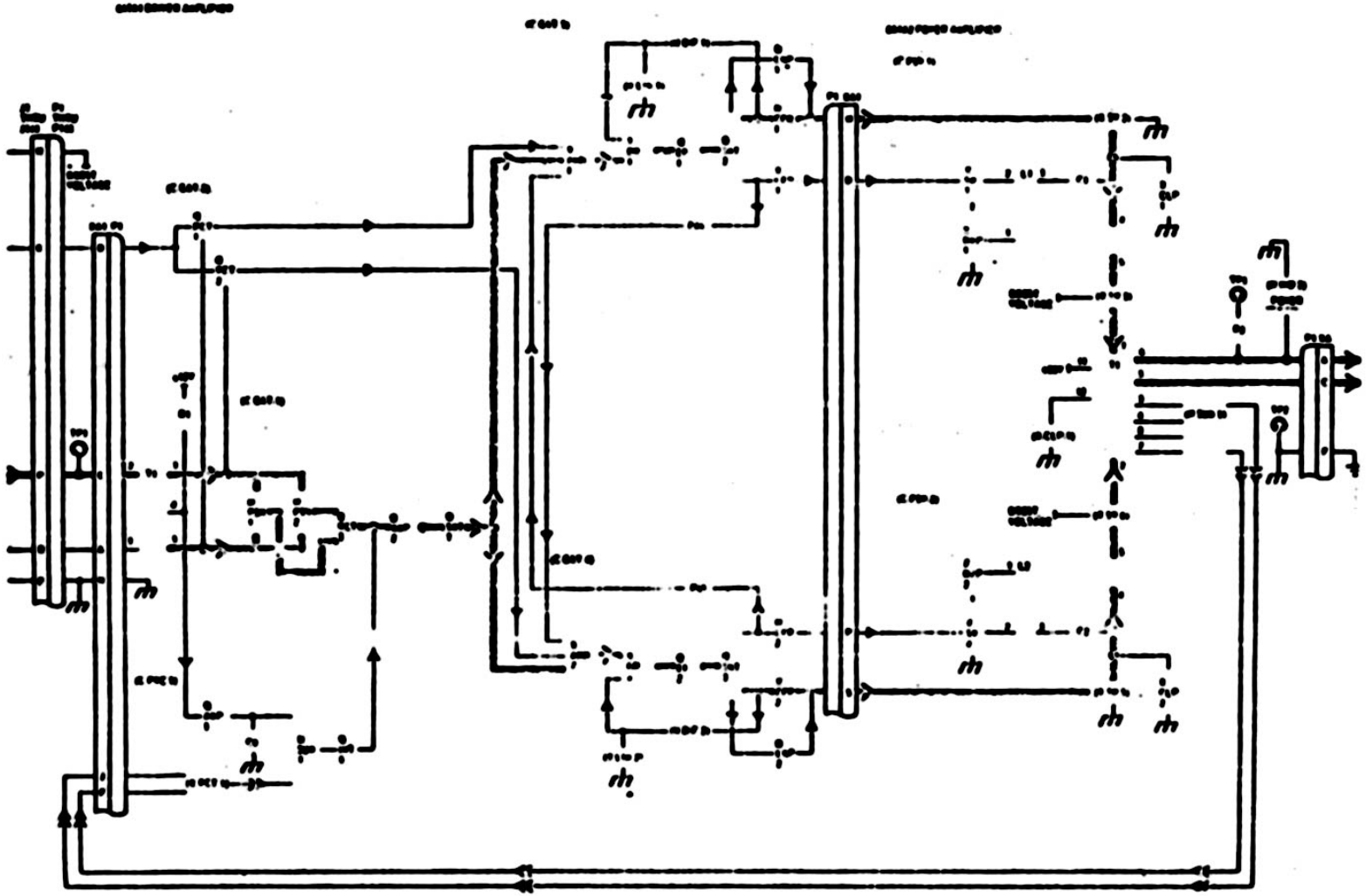
Each assembly for which a blocked schematic is prepared will have a corresponding text page. See figure 6. The physical and functional structure of the assembly shown on the text page is identical to that shown on the schematic. The schematic detail within the blue shades of the schematic is replaced by descriptive text on the blocked text page. In as few words as possible, the circuit is analyzed and described in the detail required to completely explain its operation.

For familiar and conventional circuits, identification and functional usage in the assembly is sufficient; for less familiar or unique circuits, complete analyses and descriptions are required.

As the reader progresses across the page, following the signal flow from left to right, he obtains an understanding of the operation of the total assembly in as few words as possible. At no time does he lose his place in the description, or become confused by the paragraph structure. No longer does the reader have to search through a table of contents or an index to find his subject matter. All the text concerning the assembly is immediately at hand on a page which is a replica of the schematic of that assembly.

BLOCKED TEXT FOR PRECISE ACCESS BLOCK DIAGRAMS

Each system function for which a functional block diagram is prepared has a corresponding blocked text page. The physical and functional structure shown on the text page is identical to that shown on the precise access block diagram. Only the block symbology is replaced by descriptive text. In many cases, it is only necessary to describe the major functional parts and the operation of the assembly as a whole. This is possible since the functional structure of the assembly is adequately portrayed on the



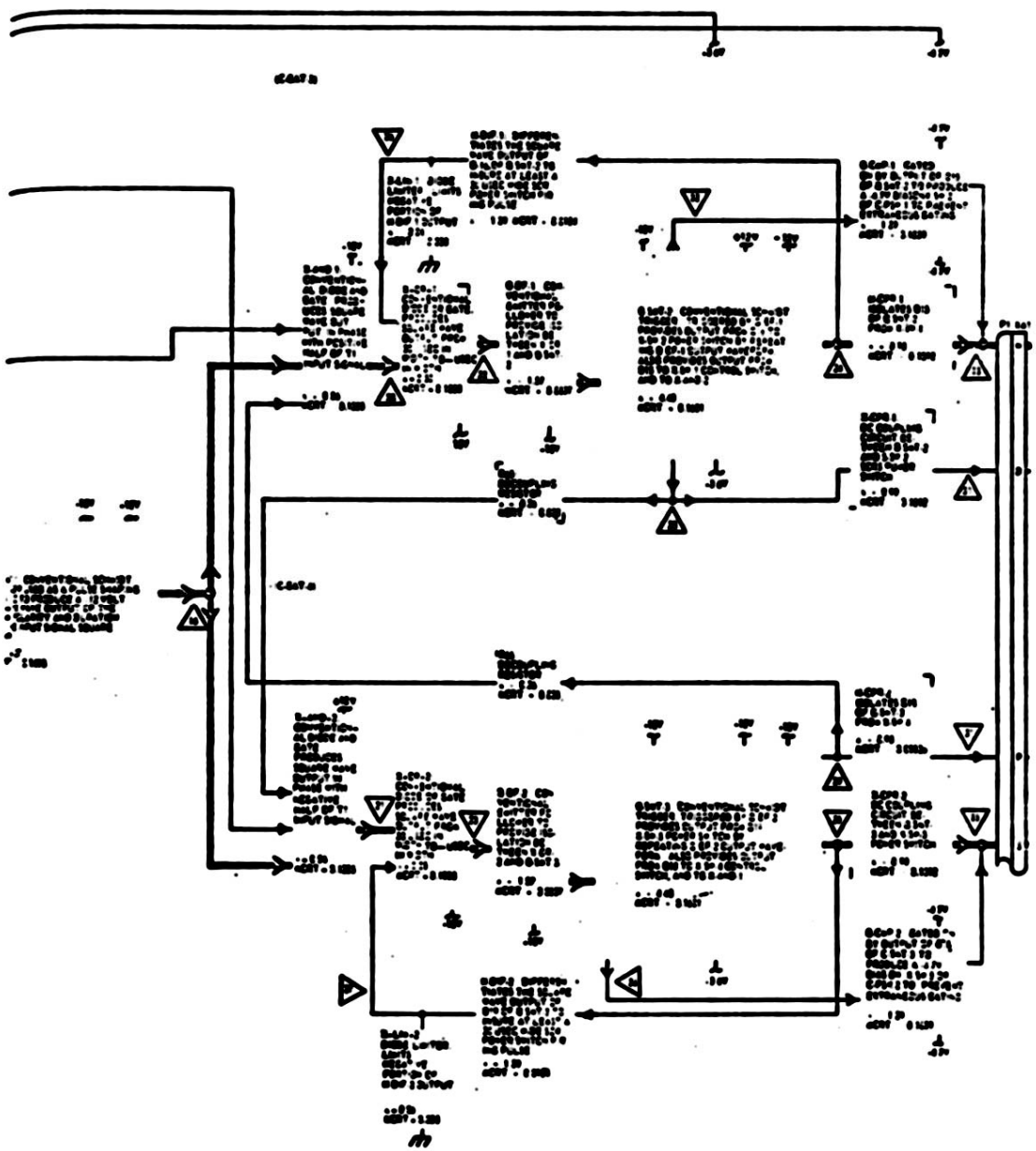


Figure 6.

precise access block diagram. Each stage is completely identified by the alphanumeric code which corresponds exactly to that of the blocked schematic and its text; therefore, if schematic detail is desired, reference can readily be made to the related blocked schematic. The blocked text format brings the total function explanation into view on a single page; thus, understanding and communication can be advanced to a degree never before possible.

The blocked text may also include figures representing such things as the calculated mean time between failures or mean time to repair for use in calculating availabilities for the function, the equipment, and the system.

BLOCKED TEXT FOR A FUNCTION

The blocked text for a function provides both a blocked diagram and the descriptive text of a function on one diagram. It is similar to the blocked text for precise access block diagrams, except that it lacks the stage-by-stage detail. It is an information tool for revealing the scheme used to mechanize the function. Since every input and output is clearly specified, the interface between this and other functions or other equipments is completely defined. The blocks at this level are primarily subfunctional groupings and the text within each block completely describes the input and output signals, but may or may not give device description. If the equipment is capable of various modes of operation, those modes are clearly specified in relation to the complete functional operation and also in relation to each subfunctional grouping operation. This defines clearly which groups of circuits work in which modes of operation and which provides a more accurate basis upon which to analyze the function. In summary, the features which make the blocked text effective as a design disclosure format are the following:

1. Al detailed text is presented on a page facing its related diagram.
2. All general text is presented within the blocks of a block diagram.
3. Physical arrangement of the text is identical to the physical arrangement of the diagram which it describes.

DESIGN OUTLINE

Finally we come to the real crux of the design disclosure format and the reason why we went through all the trouble that we just finished... the DESIGN OUTLINE. Well, what is a design outline? An outline we know should be a kind of a shorthand form of something. It is a shorthand form of how we make our notes before we make a talk like the one I am giving this morning. In the realm of hardware the design outline is a shorthand form of what we have in our equipment. Is it a circuit schematic diagram? Yes, it is. However, it uses three basic symbols, whereas our normal conception of a schematic diagram is a combination of many symbols. Today I am going to take you through the development of a Design Outline slowly. This is going to take up most of ray time, because I want you to understand a design outline. If you walk away from here with nothing else, walk away knowing that you know what a design outline is, because it is new and it is different. The design outline is a kind of philosophy. In developing it, we shall use reason, and we are not going to resort to any kind of complicated mathematical formulas.

The typical design outline is divided into four main areas as shown in figure 7. These are the chart body, headings, procedure column, and notes. The chart body presents the interdependencies of the functional elements which make up the system. The chart heading identifies the functional elements and associated input-output events. The procedure column describes the conditions or steps which are required to produce the indicated events. The notes provide detailed specifications for the input-output events indicated on the chart body. The event specifications are keyed to the output events by sequentially numbering the out-put events and using these numbers as a reference in the notes.

TYPICAL DESIGN OUTLINE FORMAT

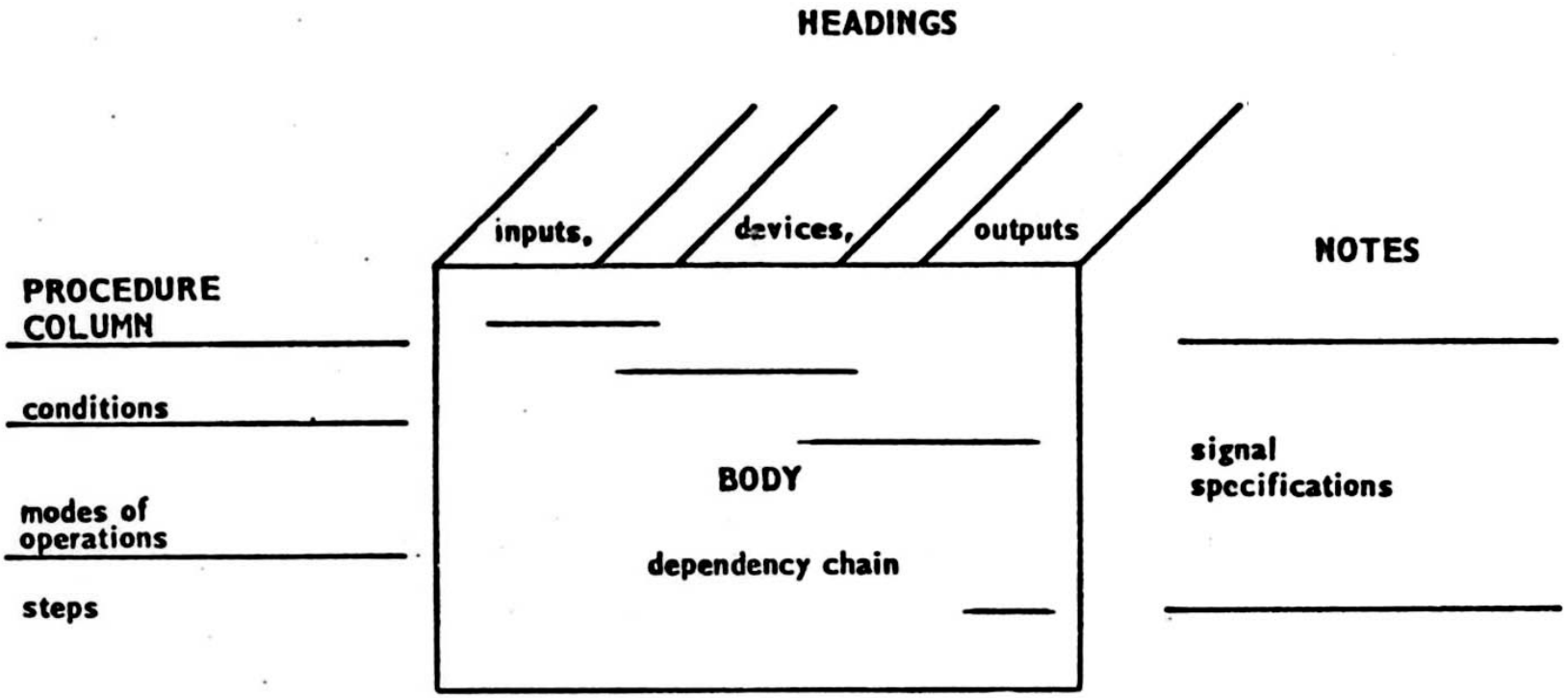


Figure 7.

The content of the logical model chart provides a distinct visibility of the equipment not attained in a block diagram presentation. Some of the factors apparent from a logical model chart that are not apparent from a block diagram approach are:

1. The design outline shows the inter-relationship of the functional elements under different modes of operation. The value of this presentation increases with an increase in the number of modes or sub modes.
2. The design outline allows comparison of the functional element involvement from mode to mode since the total structure is shown in each mode.
3. The design outline defines the man-machine interface.
4. The design outline provides detailed event specifications.
5. The design outline provides the framework for the inclusion of reliability and maintainability information.

PRINCIPLES

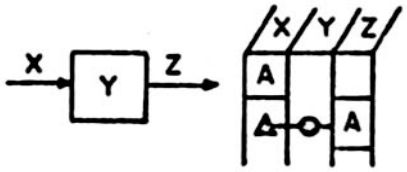
The design outline is constructed by first listing functional elements and their associated inputs and outputs on the chart heading. Then, by applying procedural information, establish the dependency of the output events upon previous events and functional elements in the form of dependency chains. A dependency chain is constructed using a logic mechanism of three basic symbols, a triangle, a dot, and a box:

△ Proof Marker which indicates a dependency on a previous event.

O Dependency Dot which indicates a dependency on functional element. Variations of the dependency dot are as follows:

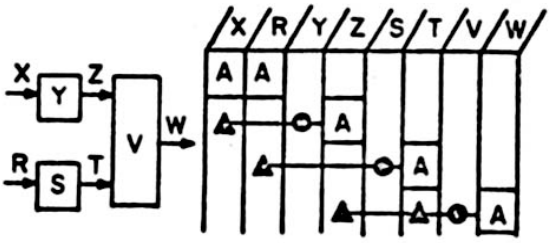
1. ◑ or ◐ indicates that functional element requires two or more events to prove correct operation.
2.  indicates a functional element which may be bypassed.
3. O/indicates relay contact set that provides continuity in de-energized state.
4. /Oindicates relay contact set that provides continuity in energized state. Event Entry which indicates an output event. Additional entries inside this symbol denote nature of event. The background of event symbol indicates ease with which event may be observed. White background de-notes events requiring access to the inside of the equipment. Black back-ground denotes events observable from front of equipment. Examples of some events are as follows:
   1.  output event available or performing within specification.
   2.  output event represents energized relay.
   3.  output event represents front panel indicator lighted.

Below is a simple dependency chain.



This example shows the dependency of output event "Z" on functional element "Y" and the presence of input event "X." If we think of Y as a blade of grass, the previous relationship can be described by saying, "if oxygen (Z) is being emitted from the blade of grass, the grass (Y) is performing its natural function, and it has the proper combination of nutrients (X) for growth."

Adding a simple circuit to our discussion, we arrived at the following dependency chains.



The dependency chains are arranged and grouped to form a symbolic representation of the operation of a functional group of equipment. Differences in the chains from mode to mode can also be shown. The output event specifications are then added to complete the Outline. Thus, through the use of a logical model, the complete interrelation-ship of functional elements and their associated output events is presented on the Design. Outline.

VARIETIES

During this talk we shall identify five varieties of design outlines. These are the System Design Outline, Prime Function Design Outline, Equipment Design Outline, Function Design Outline, and the Maintainability Disclosure Chart. These varieties were developed to ensure complete description of system design at all levels in each phase of the life cycle. The function and interrelationship of each of these design outlines may be briefly identified as follows:
A System Design Outline is used to show the relationship between equipments used in system design. At the concept phase of the life cycle, the system design outline shows all possible equipment which may perform required system prime functions. At successive phases of the life cycle, the system design outline is updated to show those equipments selected to perform the required functions.

A Prime Function Design Outline identifies the equipment associated with each prime function of the system, the major input and outputs between equipments, and the end outputs of the prime functions. It is used initially in the program definition phase and updated to reflect changes in successive phases.
An Equipment Design Outline identifies the functions of each equipment, inputs and outputs of the equipment modes of operation, and all interdependencies. It is used initially in the project definition phase and updated to reflect changes in successive phases.

A Function Design Outline identifies devices used to perform an equipment function. It is used initially in the project definition phase where the outline identifies devices and alternate schemes of devices capable of producing required functional outputs. At successive phases, the outline is updated to reflect choices of devices or changes.

Maintainability Disclosure Chart describes the complete operation of a function, identifies its equipment maintainability features, and provides a guide for optimum fault diagnosis. It is initially used in the preliminary design phase to obtain a first approximation of equipment maintainability features. It is updated in successive phases through the detailed design phase as equipment design becomes more firm. In the production phase, the maintainability disclosure charts are modified as necessary to make up the set of integrated maintenance charts which are used as a troubleshooting aid in the field maintenance manual.

All of these varieties of design outlines employ the same logical modeling principles. However, the appearance and content will change as a function of the desired level of coverage.

MAINTAINABILITY DISCLOSURE CHART

I shall restrict this discussion to the most interesting of the design outlines, the maintainability disclosure chart. (See figure P.) Examination of the maintainability disclosure chart reveals that each functional element of the blocked schematic diagram is listed in the chart heading. The unique alphanumeric coding of the functional elements provides positive correlation between the chart and the blocked schematic diagram. In general, the relative position of the functional elements in the heading, from left to right, corresponds to the position of the functional element, from left to right, on the blocked schematic diagram. The event entries associated with each functional element are listed both by entering the point at which the event may be monitored and a specification number associated

6A1 AMPLIFIER ASSEMBLY

TURN-ON AND CHECK-OUT PROCEDURE	P1-L/TP2 (-12V)	TP2 GROUND	X-VR-1	X-VR-1 (OUTPUT)/TP2 (-3.6V)	P1-N TP2 (-12V)	X-VR-2	X-VR-2 (OUTPUT) TP2 (-4.7V)	TP3 TP2 (SIG. IN)	T1	R1	T1-3/5	Q-RCT-1	Q-RCT-2	T1-4/TP2	C9	Q-AMP-1	Q3-C/TP2	XA1-J/F	X-RCT-1	JUNCTION R32, R33/TP2	N-PSH-1	Q1-B-TP2	N-PSH-2
ESTIMATED MEASUREMENT TIME/[A] ESTIMATED DIAGNOSIS TIME ●	0.01	0.01	0.406	0.01	0.01	0.364	0.01	0.034	0.518	0.518	0.034	0.562	0.562	0.034	0.580	0.584	0.034	0.034	0.454	0.034	0.496	0.034	0.454
MEAN CIRCUIT REPAIR TIME (MCRT)			0.049			0.064			0.154	0.028		0.077	0.077		0.028	0.092			0.153		0.083		0.083
CIRCUIT FAILURE RATE (λ)			2.34			3.06			1.25	0.36		1.21	1.21		0.57	1.93			0.60		0.93		0.93
ESTIMATED REPAIR TIME (ERT)			0.455			0.428			0.672	0.546		0.639	0.639		0.608	0.676			0.607		0.579		0.537
INCREMENTAL REPAIR TIME (IRT)			0.011			0.014			0.009	0.002		0.008	0.008		0.004	0.014			0.004		0.006		0.005
SIGNAL SPECIFICATION	1	2		3	4		5	6			7			8			9	10		11		12	
REMOVE LEADS AT XA1-J/F. INSERT AT XA1-J/F A SINE WAVE INPUT SIGNAL AT FREQUENCY OF ___ AND PEAK TO PEAK AMPLITUDE OF ____.	A	A		A	A		A	A			A			A			A	A		A		A	

1. -12V
2. GROUND
3. -3.6V
4. -12V
5. -4.7V

6.

7. SAME AS 6

8. SIGNAL IN PHASE WITH 6.

9. V

10.

11. V

12. LEADS 6 BY 90°

with each event. The specification numbers are then listed in the notes with the corresponding detailed event specification.

The chart body portrays the dependency chain structure as the inputs are processed through the functional elements to develop the desired outputs. The complex interrelationships are clearly and precisely defined. The chart represents the functional design of the Amplifier Assembly summarized in such a fashion that now an organized approach to the maintainability design may be made.

If the body of the chart defines the involvement of each functional element in the total dependency chain of event availabilities, then it clearly follows that the failure of any functional element will be revealed by the absence of availabilities dependent upon the failed element. If the total pattern of event availabilities could be known immediately, the isolation of a fault to the failed element would be no problem. The visibility provided by the chart would clearly reveal that only one functional element could produce that particular availability pattern. In practice, the measurement of event availabilities in terms of event specifications takes time and must be performed sequentially. From the starting point of front panel indications, reference to the chart reveals the fault lies between the first bad indication and the last good indication. The chart then establishes the next logical internal measurement. From the information gained on the chart, we can determine successive measurements required to .isolate to the fault. When the chart is used in the maintainability prediction process, we can assume a failure, determine the availability pattern and develop the optimum diagnosis sequence. With this established, the time required to isolate and repair that failed element can be calculated. The maintainability disclosure chart provides a format for the summary for these calculations for each function element.

The maintainability information is presented in five additional headings at the top of the chart. These five headings contain:

An Estimated Measurement Time and Estimated Diagnosis Time. An estimated measurement time is entered for each event entry and is the time necessary to test for the proper output at an event entry.

An estimated diagnosis time is entered for each functional element and is the time necessary to isolate a failure to a functional element on the chart.

The Mean Circuit Repair Time (MCRT). An MCRT, which is calculated and entered for each functional element, is the time necessary to locate, remove, and replace a faulty part within an isolated functional element.

The Estimated Repair Time (ERT). An ERT, calculated and entered for each functional element, represents the total time to restore a failed functional element to opera-Ron. An important point to remember is that the ERT is the sum of the diagnosis time and the MCRT.

A Functional Element Failure Rate (A). These failure rates are calculated and entered for each functional element on the chart. The failure rates are in terms of failures per 10' hours. The sum of the functional element failure rates is entered at the end of this heading along with its reciprocal which represents the chart function mean time between failures (MTBF).

An Incremental Repair Time (IRT). This IRT is calculated and entered for each functional element. It represents the portion of the total mean time to repair (MTTR) contributed by that functional element. The IRTs are summed and entered at the end of this heading to provide mean time to repair (MTTR) for the functional elements on the chart.

With data accumulated for each function-al element and the total function, we can proceed to an analysis of the function from the maintainability point of view. At this level the presentation reveals all of the critical maintainability features of the equipment. The event entries on the chart reveal

the possible location of event sensors. Analysis of the associated maintainability data reveals the effectiveness of various packaging schemes.

Thus, the logical model presentation and maintainability data provides clear and accurate means of determining effective equipment design with maximum maintainability.

DATA PRESENTATION

Maintainability information, as opposed to reliability data includes expressions of human effort and capability. The maintainability information presented on the maintainability disclosure chart is personnel and time oriented but is keyed to part and functional element failure probability in such a manner that the effects of a change in any parameter upon part failure rate and maintainability can be readily seen. The calculation mechanics are straightforward and are of the form which is readily adaptable to automatic data processing. Trial parameter changes can be introduced either manually or by automatic data processing to note the effects on other parameters.

The maintainability disclosure chart lay-out and its data acquisition and display agrees with certain general criteria for design of maintainability prediction and disclosure system. Some of these criteria are:

1. It should be clear, concise, and understandable to the user.
2. It should be based on information available to the user.
3. It should produce similar outputs when manipulated by independent workers.
4. It should require only simple and rapid forms of mathematical manipulation.
5. It should consider and deal effectively with all interfaces to any maintainability parameter.
6. It should be immediately responsive to any parameter change, either real or simulated.
7. It should provide outputs which are time, resource, and probability oriented.
8. It should be useful through the various decision and development phases of a system.
9. Its predictions should agree with maintainability data observed on the actual equipment.

Data is obtained, entered on the maintainability disclosure chart, and manipulated to produce output information to be evaluated by your program managers. Source data will be organized in a set of data catalogs, derived from existing sources and future time and motion studies. The body of the chart provides the framework for the calculation of diagnosis times, mean circuit repair time, estimated repair time, relative failure frequency, incremental repair time for each functional circuit element. Incremental repair times for all circuits are summed to provide function MTTR. Summation of the circuit failure rates provides the function failure rate, which is inverted to provide a function mean time between failures (MTBF).

The maintainability disclosure chart lay-out and its data following maintainability information is entered on the chart: measurement times, diagnosis times, mean circuit repair times, estimated repair times, circuit failure rates, incremental repair times MTTR, total failure rate, and MTBF.

MAINTAINABILITY ANALYSIS

The design disclosure formats are a set of specialized documents designed to define electronic systems at all levels, tie together all pertinent design information, and present all relevant fundamental data. The formats organize systems in a manner that facilitates analysis. The formats are not, in themselves, the analyses but are the tools for conducting analyses.

One great value of the design disclosure formats is that the discipline of this documentation scheme permits analyses to be formalized. In other words, we can devise procedures for studying various system characteristics. These procedures we refer to as analytic techniques.

Some typical analytic techniques would reveal:

1. The distribution of downtimes
2. The distribution of relative failure frequencies
3. The need for diagnostic sensors vs. functional modularization
4. The optimum test point locations
5. The optimum location of front panel indicators
6. The test equipment requirements and relative frequency of use
7. Personnel skill requirements

Analytic techniques may be devised in as many areas as maintainability questions may be asked.

Let us first examine the distribution of downtimes. Figure 9 provides an exhibit of a distribution constructed on a portion of a sonar equipment.

The distribution is derived from data on the maintainability disclosure chart. Fixed intervals of repair time are established, then the relative failure frequencies are summed for the estimated repair times that fall within those intervals.

A study of the distribution reveals some interesting characteristics. For example, no estimated repair times are greater than 0.70 hours or smaller than 0.20 hours. The largest percentage of failures is found in the interval from 0.60 hours to 0.70 hours.

It is further obvious that the distribution is neither normal or log-normal as might be typically assumed. We see a strong discontinuity in the longer repair times. Traceability as to the contributors to this discontinuity is provided by simply scanning the data rows of the chart for those elements with an ERT in the interval 0.65 to 0.70.

In certain situations, the quantitative maintainability requirements may be expressed in terms of the component parts of MTTR. For example, the qualitative statement "maximum use of fault isolation design techniques shall be made so as to reduce fault diagnosis time" could be expressed quantitatively as "the mean of diagnosis times shall not exceed 4.0 hours." Similarly, the qualitative statement "good construction practices shall be employed to facilitate circuit repair" could be expressed quantitatively as "the mean of circuit re-pair times shall not exceed 2,0 hours." In this fashion, we can not only specify the desired equipment MTTR, but also we can specify the manner in which the desired MTTR is to be accomplished. Thus the complete specification could be:

MTTR =	**MEAN OF ESTIMATED REPAIR TIMES**	**= MEAN OF DIAGNOSIS TIMES**	**+ MEAN OF CIRCUIT REPAIR TIMES**
MTTR =	**6.0 HOURS**	**= 4.0 HOURS**	**+ 2.0 HOURS**

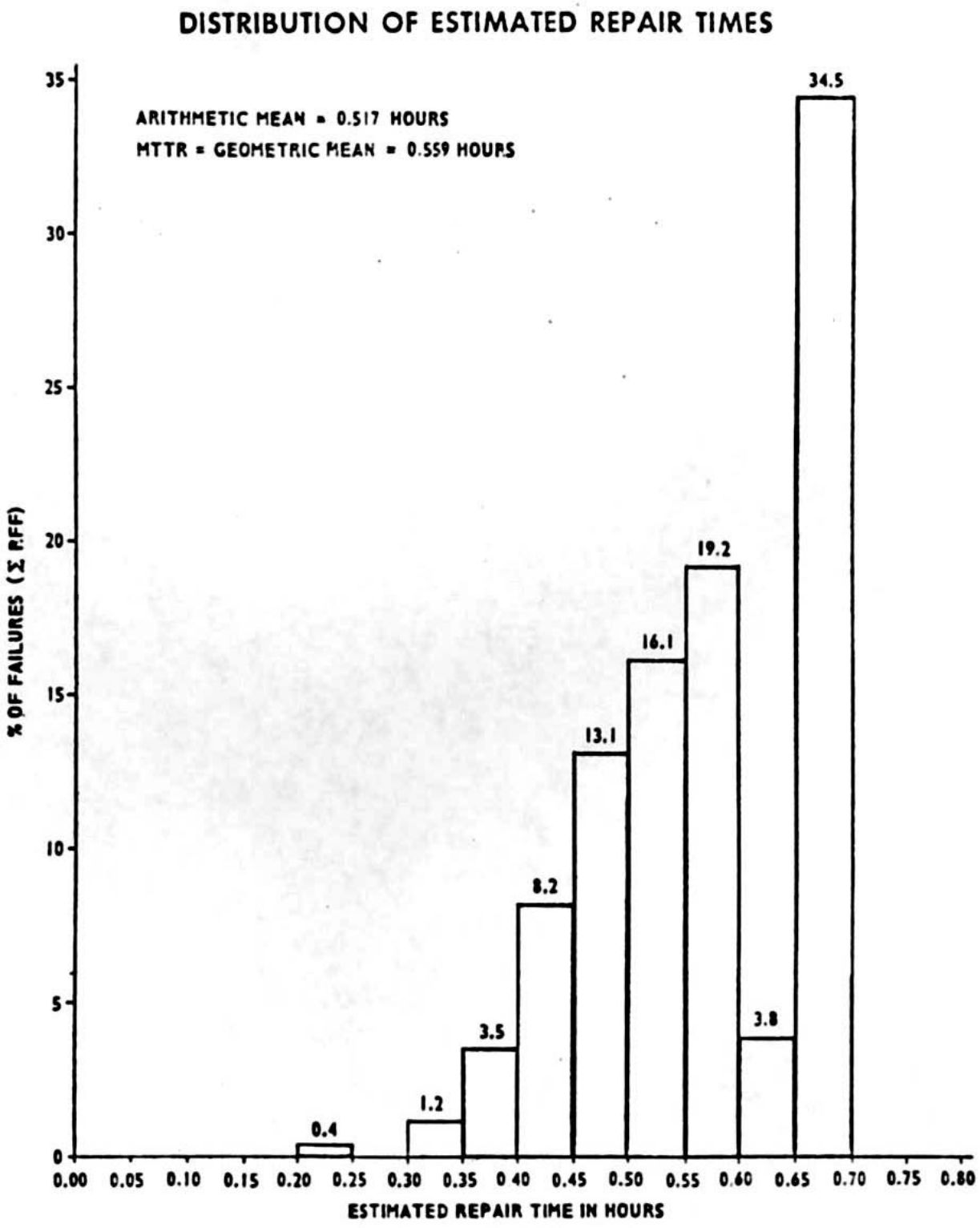

DISTRIBUTION OF ESTIMATED REPAIR TIMES
ARITHMETIC MEAN = 0.517 HOURS
MTTR = GEOMETRIC MEAN = 0.559 HOURS
% OF FAILURES (Σ RFF)
ESTIMATED REPAIR TIME IN HOURS
0.4
1.2
3.5
8.2
13.1
16.1
19.2
3.8
34.5
0
5
10
15
20
25
30
35
0.00 0.05 0.10 0.15 0.20 0.25 0.30 0.35 0.40 0.45 0.50 0.55 0.60 0.65 0.70 0.75 0.80

Figure 9.

The factors of diagnosis and repair can also be represented by distributions constructed from chart data.

From figure 10, we can see that no diagnosis time exceeds 0.60 hours or is less than 0.10 hours. The interval with the largest percentage of failure is between 0.30 hours and 0.35 hours. We can see that the cumulative distribution is relatively smooth and free of discontinuities. This type of continuous distribution at the equipment level would tend to show that a consistent fault isolation philosophy has been used in the design process.

From figure 11, we can see that no circuit repair time exceeds 0.35 hours. The interval with the largest percentage of failures is between 0.30 hours and 0.35 hours, and there are no circuit repair times between 0.20 hours and 0.30 hours. It is significant to note the large and disjoint contribution of the last interval. A discontinuous distribution such as this at the equipment level would indicate an inconsistent circuit design philosophy.

Up to this point, we have concentrated upon providing project management, both contractor and government, with the assurance that the quantitative maintainability requirements have been met. We now turn our attention toward motivating the designer. Our desire is to point out those areas in which additional maintainability design efforts will yield significant benefits in terms of reduced MTTR.

The first step is to array the circuits in order of descending incremental repair times (IRT). This will reveal the relative contributions of each to the =TR. In figure 12 circuits 37 and 38 dominate the distribution. Also the next six circuits, 39, 41, 23, 24, 15 and 16 have incremental repair times well above the rest of the distribution. Circuits 37 and 38 together total 0.197 hours, or 35c; of the MTTR of 0.559 hours. The next six circuits total 0.159 hours, or 28% of the MTTR. Thus, taken together, these eight circuits, 19 percent of the 42 total circuits, account for 63 percent of the MTTR. Obviously then, if significant reduction is to be made in the MTTR, maintainability design effort should be concentrated on these eight circuits. This point should be made absolutely clear. Since all of the circuits contribute to the MTTR, a reduction of any incremental repair time will reduce the MTTR. However, if we assume a dollar constraint or a time constraint, we are forced to concentrate our efforts where the greatest potential benefits will be derived.

To determine a course of action at this point, we could examine the components of incremental repair time: The diagnosis time increment and the MCRT increment. The distributions for these increments are shown on the next two figures, 13 and 14. Here we notice two facts. The diagnosis time increments are consistently larger than the corresponding MCRT increments, and the first eight columns in each of the three distributions involve the same eight circuits, although their order changes somewhat. From the first observation, it is evident that the maintainability design effort should be concentrated primarily on the reduction of diagnosis times. From the second observation, it can be deduced that these circuits have high relative failure frequencies. This fact is borne out in figure 15 which shows the distribution of relative failure frequencies. Here we observe that the first eight columns again involve these same eight circuits. Significant reductions in MTTR would result if the failure rates of these circuits could be reduced. Close coordination is required between the maintainability and reliability design efforts if the trade off is to yield the maximum benefit.

In actual practice, the designer can plot his course of action from the table of calculations without preparing the full illustration of the distribution. Once the general shape of the distribution is grasped and the implications understood, design motivation should follow as a natural consequence. However, it should be noted that

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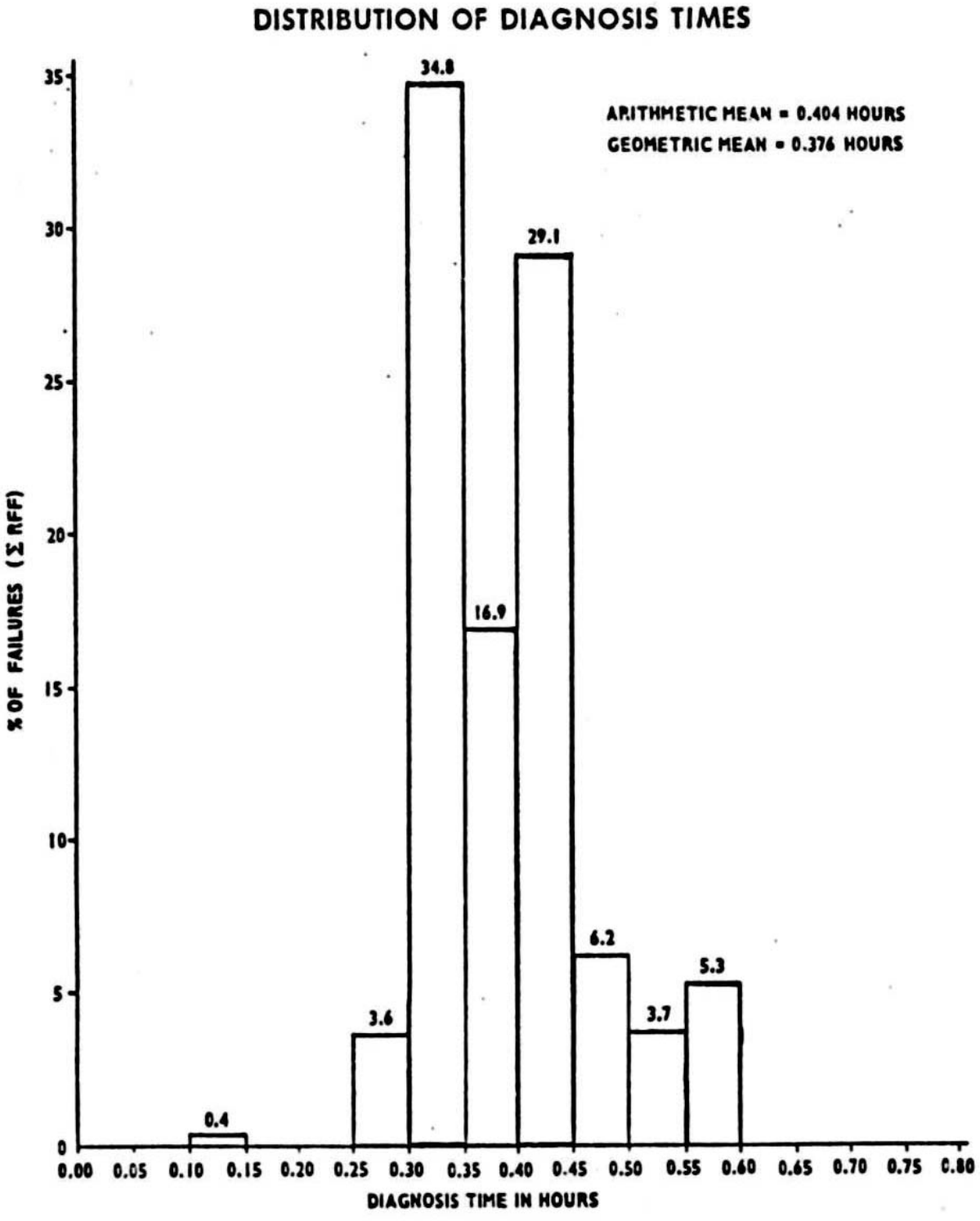
DISTRIBUTION OF DIAGNOSIS TIMES
ARITHMETIC MEAN = 0.404 HOURS
GEOMETRIC MEAN = 0.376 HOURS
% OF FAILURES (Σ RFF)
DIAGNOSIS TIME IN HOURS
0.4
3.6
34.8
16.9
29.1
6.2
3.7
5.3
0
5
10
15
20
25
30
35
0.00 0.05 0.10 0.15 0.20 0.25 0.30 0.35 0.40 0.45 0.50 0.55 0.60 0.65 0.70 0.75 0.80

Figure 10.

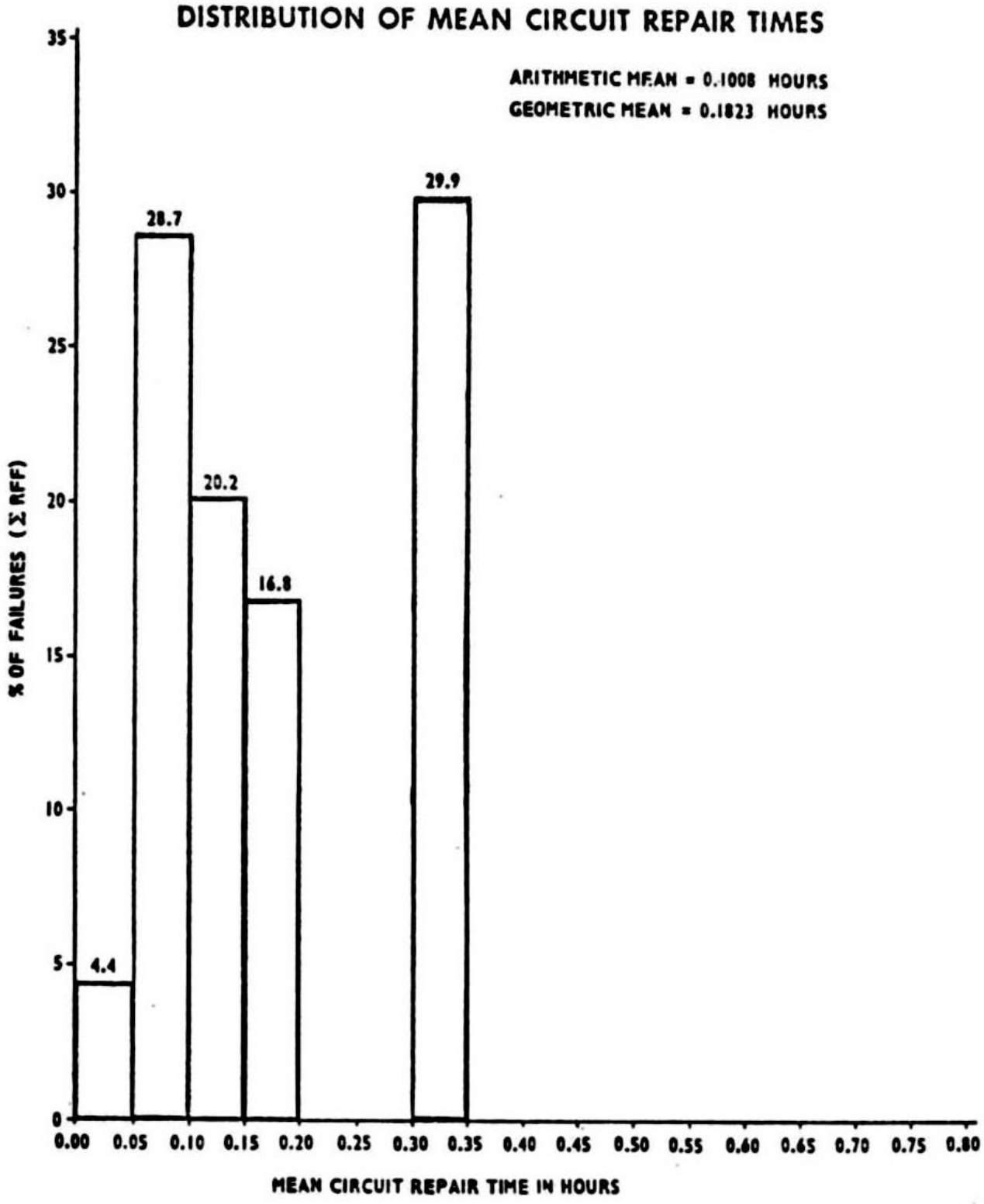
DISTRIBUTION OF MEAN CIRCUIT REPAIR TIMES
ARITHMETIC MEAN = 0.1008 HOURS
GEOMETRIC MEAN = 0.1823 HOURS
% OF FAILURES (Σ RFF)
MEAN CIRCUIT REPAIR TIME IN HOURS
4.4
28.7
20.2
16.8
29.9
0
5
10
15
20
25
30
35
0.00
0.05
0.10
0.15
0.20
0.25
0.30
0.35
0.40
0.45
0.50
0.55
0.60
0.65
0.70
0.75
0.80

Figure 11.

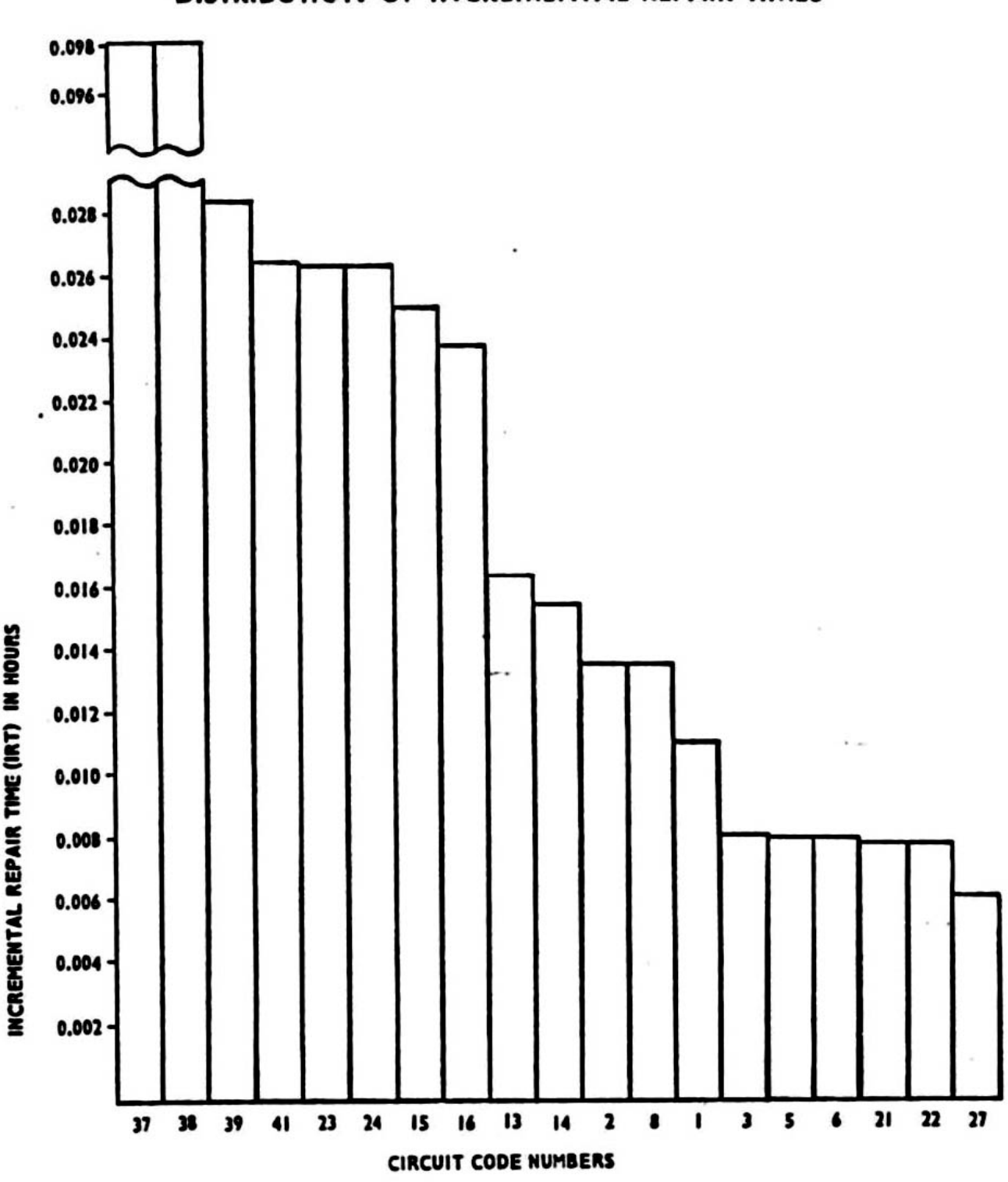
DISTRIBUTION OF INCREMENTAL REPAIR TIMES
INCREMENTAL REPAIR TIME (IRT) IN HOURS
0.098
0.096
0.028
0.026
0.024
0.022
0.020
0.018
0.016
0.014
0.012
0.010
0.008
0.006
0.004
0.002
37 38 39 41 23 24 15 16 13 14 2 8 1 3 5 6 21 22 27
CIRCUIT CODE NUMBERS

Figure 12.

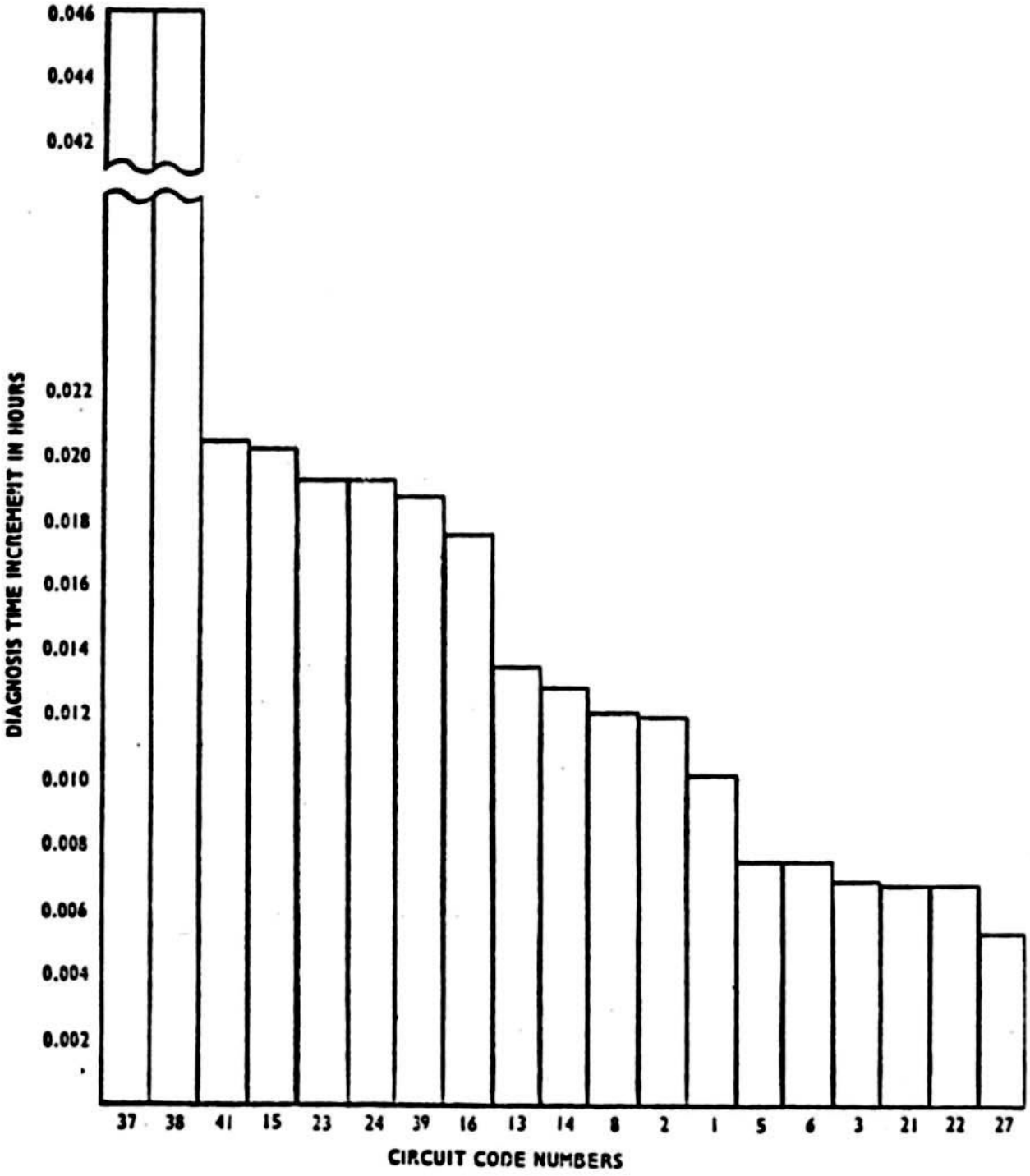
DISTRIBUTION OF DIAGNOSIS TIME INCREMENTS
DIAGNOSIS TIME INCREMENT IN HOURS
0.046
0.044
0.042
0.022
0.020
0.018
0.016
0.014
0.012
0.010
0.008
0.006
0.004
0.002
37 38 41 15 23 24 39 16 13 14 8 2 1 5 6 3 21 22 27
CIRCUIT CODE NUMBERS

Figure 13.

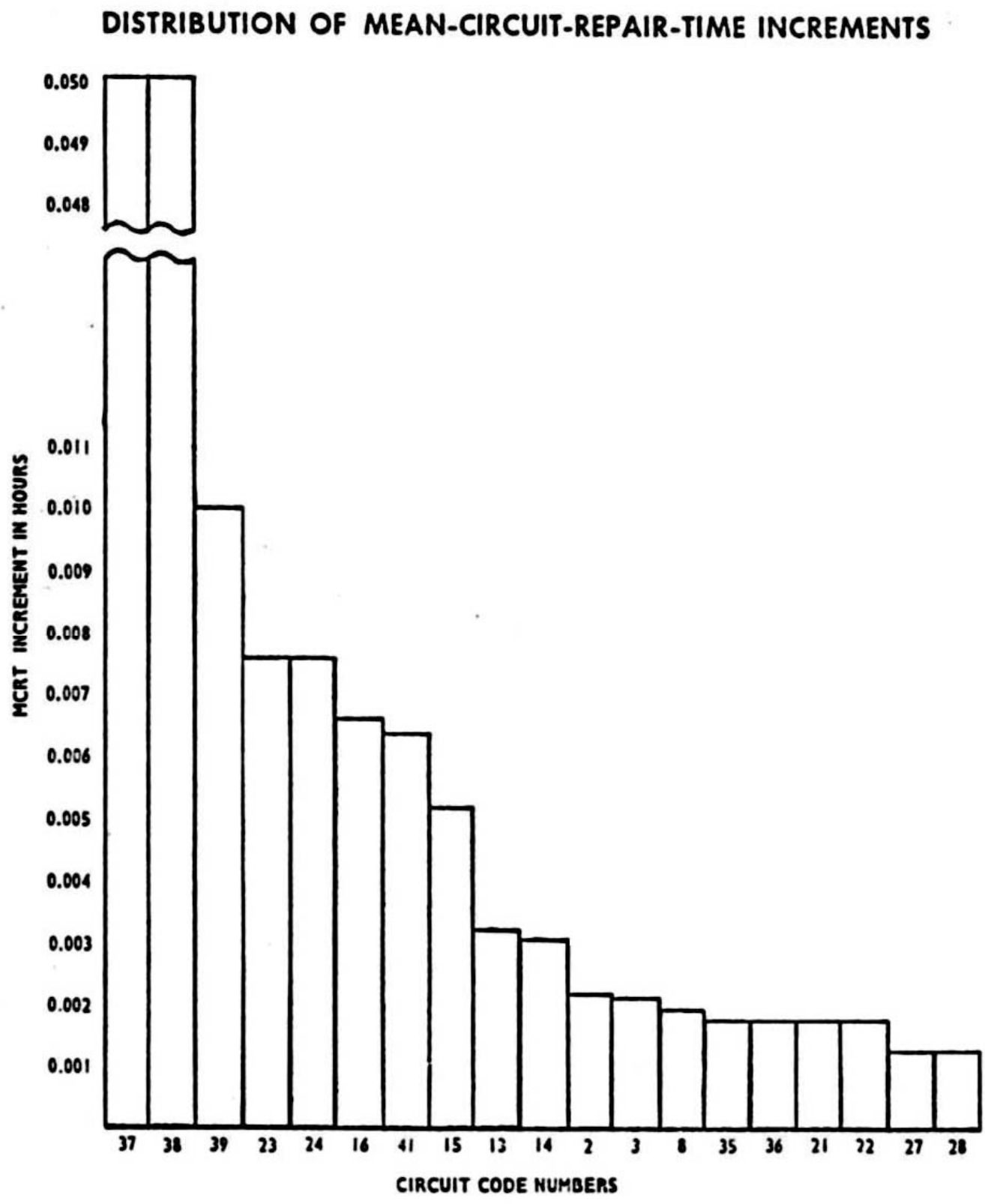
DISTRIBUTION OF MEAN-CIRCUIT-REPAIR-TIME INCREMENTS
MCRT INCREMENT IN HOURS
0.050
0.049
0.048
0.011
0.010
0.009
0.008
0.007
0.006
0.005
0.004
0.003
0.002
0.001
37 38 39 23 24 16 41 15 13 14 2 3 8 35 36 21 22 27 28
CIRCUIT CODE NUMBERS

Figure 14.

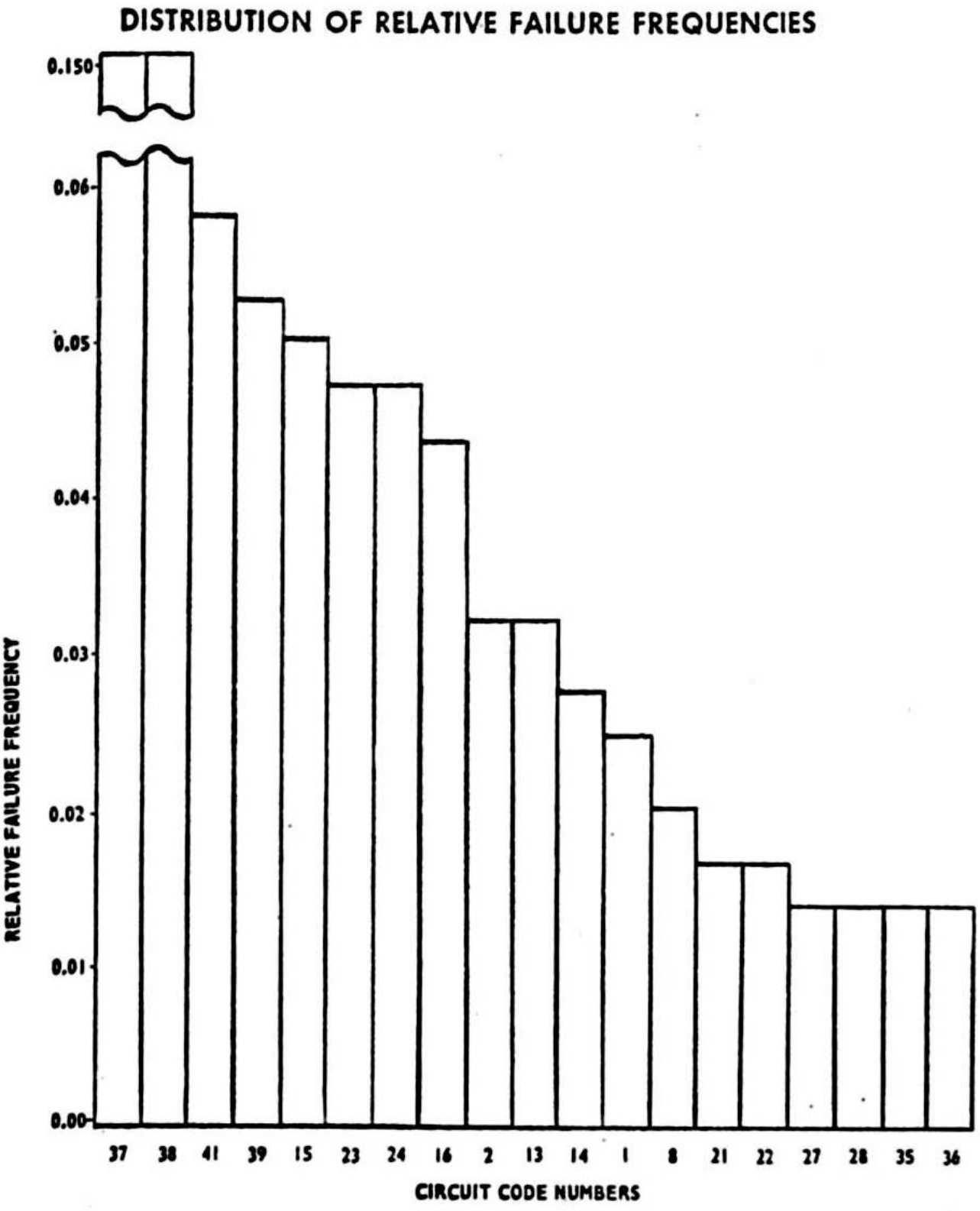
DISTRIBUTION OF RELATIVE FAILURE FREQUENCIES
RELATIVE FAILURE FREQUENCY
0.150
0.06
0.05
0.04
0.03
0.02
0.01
0.00
37 38 41 39 15 23 24 16 2 13 14 1 8 21 22 27 28 35 36
CIRCUIT CODE NUMBERS

Figure 15.

the designer can be spurred into action by specification requirements on the nature of the distribution, or by a requirement for explanation of the actions taken to reduce significant incremental times.

We have seen that the statistical analysis of design can yield more than a paper estimate of .MTTR. The examination of the various distributions has revealed several criteria that can be used with MTTR as specification requirements, or as supporting documentation. Under these criteria, the designer can see the direct effects of his maintainability decisions. Finally, project management can be assured that maintainability has been designed into the equipment as a result of conscious directed efforts.

Now, let us examine another way in which analytic techniques may be used in design. The selection of monitoring points for the purpose of sensing equipment performance has always been a subjective process. This is particularly true at the lower hardware levels where minor signals are involved or where major system outputs are in an intermediate stage of development. The desirability of adequate test points is well known but often the number of test points employed is left to the discretion of the individual designer.

Knowledge of the circuit-signal dependency chain leads to the derivation of the optimum fault isolation sequence for each circuit element, and thereby establishes the desired signal monitoring points. Examination of the monitoring point usage for all the circuit isolation sequences and consideration of the relative failure frequency of each circuit will forecast the frequency of use of each monitoring point. Using predetermined trade-off criteria, an objective procedure for test point selection can be employed.

A test point matrix, as shown in figure 16, provides a useful tool for this analysis. This matrix lists the candidates for test points across the top and the circuits that may fail along the left. Each circuit in turn is assumed to fail and "Xs" placed to identify the test locations that would be used. When this process is complete, we can easily see which test locations are used most frequently by the number of Xs entered in the respective columns.

This must be further amended to provide for the differences in failure frequency of the circuits involved. For this reason, the relative failure frequency (RFF) is entered for each circuit at the left. The relative usage of each test location is given by the sum of the relative failure frequencies of all the circuits checked in its column.

The relative usage frequency of the test point candidates is the measure of their desirability as design features. Hence, we can assemble an ordered listing of the test points to be selected as shown in figure 17. This table shows that monitoring point 45 would be used 100% of the time, 41 would be used 99% of the time, and so on.

Now, we might ask, what is the MTTR benefit realized by the incorporation of each test point. Studies could reveal that, for example, the addition of a test point saves the maintenance technician an average of one (1) minute (.017 hours) per test.

If we multiply this by the relative usage factor, we get precisely the MTTR improvement that would be obtained. This is provided in the fourth column. The fifth column simply states the cumulative benefit accrued. Thus the MTTR is reduced to 0.017 hours by the addition of the most desirable test point. 0.034 hours by the first two, and so on.

The last column simply gives this improvement in terms of percentage of the total improvement possible. As can be seen, the greatest improvement is realized by the first test points added. The benefit rapidly decreases as more are added.

Now we have only to introduce economics into the picture. Assume that a study has revealed the cost of a test point to be $1.00. What improvement can be made in the MTTR by spending $5.00 on test points? The answer is simply the cumulative MTTR improvement for the first five test points.

TEST POINT USE MATRIX

CKT CODE	RFF	MONITOR PT CODE																																	
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36
1	0.0251	X	X	X																				X		X								X		X	
2	0.0328		X		X	X																											X	X			
3	0.0134							X					X	X		X	X																X		X	
4	0.0039							X					X	X		X	X																X		X	
5	0.0130							X	X								X		X		X		X		X								X		X	
6	0.0130							X	X								X			X		X		X		X								X		X	
7	0.0061							X	X	X		X			X	X	X																	X		X	
8	0.0207							X	X	X		X			X	X	X																	X		X	
9	0.0064							X				X			X	X	X																	X		X	
10	0.0100					X		X					X	X		X	X																	X		X	
11	0.0100					X		X						X		X	X																	X		X	
12	0.0077							X		X		X				X	X																	X		X	
13	0.0328							X							X	X	X																	X		X	
14	0.0282					X							X	X		X	X																	X		X	
15	0.0503					X										X	X																	X		X	
16	0.0437					X										X	X																	X		X	
17	0.0060																X		X		X		X		X					X				X		X	
18	0.0060																X			X		X		X		X			X					X		X	
19	0.0054																				X		X		X		X							X		X	
20	0.0054																					X		X		X		X						X		X	
21	0.0168			X																			X		X									X		X	
22	0.0168			X																				X		X								X		X	
23	0.0475			X																			X		X									X		X	
24	0.0475			X																				X		X								X		X	
25	0.0006																								X		X								X			
26	0.0006																									X		X								X	
27	0.0138																							X			X							X			
28	0.0138																									X		X								X	
29	0.0039																X		X		X		X		X					X				X		X	
30	0.0039																X			X		X		X		X			X					X		X	
31	0.0100																											X			X			X			
32	0.0100																													X		X				X	
33	0.0106																								X									X			
34	0.0106																									X										X	
35	0.0138																																X	X			
36	0.0138																																		X	X	
37	0.1495																														X			X			
38	0.1495																															X				X	
39	0.0532																															X				X	
40	0.0116																																				
41	0.0580																															X				X	
42	0.0039																																				
		0.0251	0.0579	0.1537	0.0328	0.2076	0.0000	0.1370	0.0528	0.0345	0.0000	0.0409	0.0555	0.0655	0.0737	0.2332	0.2790	0.0000	0.0229	0.0229	0.0783	0.0283	0.0926	0.1172	0.1176	0.1427	0.0198	0.0198	0.0199	0.0199	0.1595	0.2707	0.0466	0.6746	0.0138	0.7530	0.0000

Σ RFF

Figure 16.

TEST POINT SELECTION BY MTTR IMPROVEMENT

RANK ORDER	MONITOR PT. CODE	Σ RFF	MTTR IMPROV.	CUM. MTTR IMPROV.	% of POSSIBLE IMPROV.
I	45	1.0000	0.017	0.017	15
2	41	0.9961	0.017	0.034	30
3	35	0.7530	0.013	0.047	42
4	33	0.6746	0.011	0.058	52
5	40	0.5034	0.008	0.066	59
6	16	0.2790	0.005	0.071	63
7	31	0.2707	0.005	0.076	68
8.	15	0.2332	0.004	0.080	71
9	5	0.2026	0.003	0.083	74
10	30	0.1595	0.003	0.086	77
II	3	0.1537	0.003	0.089	79
12	25	0.1427	0.002	0.091	81
13	7	0.1370	0.002	0.093	83
14	23	0.1177	0.002	0.095	85
15	24	0.1176	0.002	0.097	87
16	22	0.0926	0.002	0.099	88
17	14	0.0737	0.001	0.100	89
18	13	0.0655	0.001	0.101	90
19	2	0.0579	0.001	0.102	91
20	12	0.0555	0.001	0.103	92
21	8	0.0528	0.001	0.104	93
22	32	0.0466	0.001	0.105	94
23	II	0.0409	0.001	0.106	95
24	9	0.0345	0.001	0.107	96
25	4	0.0328	0.001	0.108	96
26	20	0.0283	0.000		
27	21	0.0283			
28	I	0.0251			
29	18	0.0229			
30	19	0.0229			
31	28	0.0199			
32	29	0.0199			
33	26	0.0198			
34	27	0.0198			
35	34	0.0138			
36	44	0.0016			
37	6	0.0000			
38	10	0.0000			
39	17	0.0000			
40	36	0.0000			
41	37	0.0000			
42	38	0.0000			
43	39	0.0000			
44	42	0,0000			
54	43	0.0000			

Figure 17.

BENEFIT IN DOLLARS		MTTR IMPROVEMENT INCREMENT IN HOURS		MARGINAL REVENUE RATIO IN DOLLARS PER HOUR
TEST POINT	1	$1.70	0.017 HOURS x	$1 / 0.010 HOURS
	2	$1.70	0.017 HOURS x	$1 / 0.010 HOURS
	3	$1.30	0.013 HOURS x	$1 / 0.010 HOURS
	4	$1.10	0.011 HOURS x	$1 / 0.010 HOURS
	5	$O.8O	0.00S HOURS x	$1. / 0.010 HOURS

The method just described raises additional questions. Are the costs acceptable? Are the benefits derived sufficient? These questions can be answered using a marginal cost-marginal revenue concept. Assume that from an economic study it can be deter-mined that each decrease of 0.010 hours in the assembly MTTR is worth $1.00 to the user. Under the marginal cost-marginal revenue concept, test points should be added up to the point where the marginal cost ($1.00 per test point) is equal to the marginal revenue ($1.00 per 0.010 hours). It can be seen that the first four test points each meet this criterion; but the fifth test point does not.

Thus if test point 5 were to be added, it would cost $1.00 and would yield a benefit of only $0.80. This is obviously an uneconomic decision. Therefore, under this contract, only the first four test points would be added.

The Design Disclosure Format concept represents a new approach to the technical information system that supports the acquisition of effective and compatible electronic systems. It promises to shed new light on system design. Today we have limited the discussion to maintainability. However, we are at present conducting research to expand the applicability to other systems effectiveness characteristics, such as reliability, operability, supportability and performance.

With the fundamental format structure developed and the maintainability techniques refined, we are ready to initiate concentrated study and development in the other areas required to supplement the existing work.

Formatting methods and analytic techniques constitute the basic concept. These have been kept general and flexible to permit broad application. Each systems development program must be studied to determine the particular requirements suited to its own purpose.

The DDF Concept is at the threshold of implementation. To accomplish this, general principles must be extrapolated into specific requirements. This is the approach that will be employed to translate the basic theory into effective practice.

We must accelerate this transition so that Navy systems development programs may realize the benefits of this concept at the earliest time possible.