Systems Approach
To
Effective Diagnostics & Prognostics

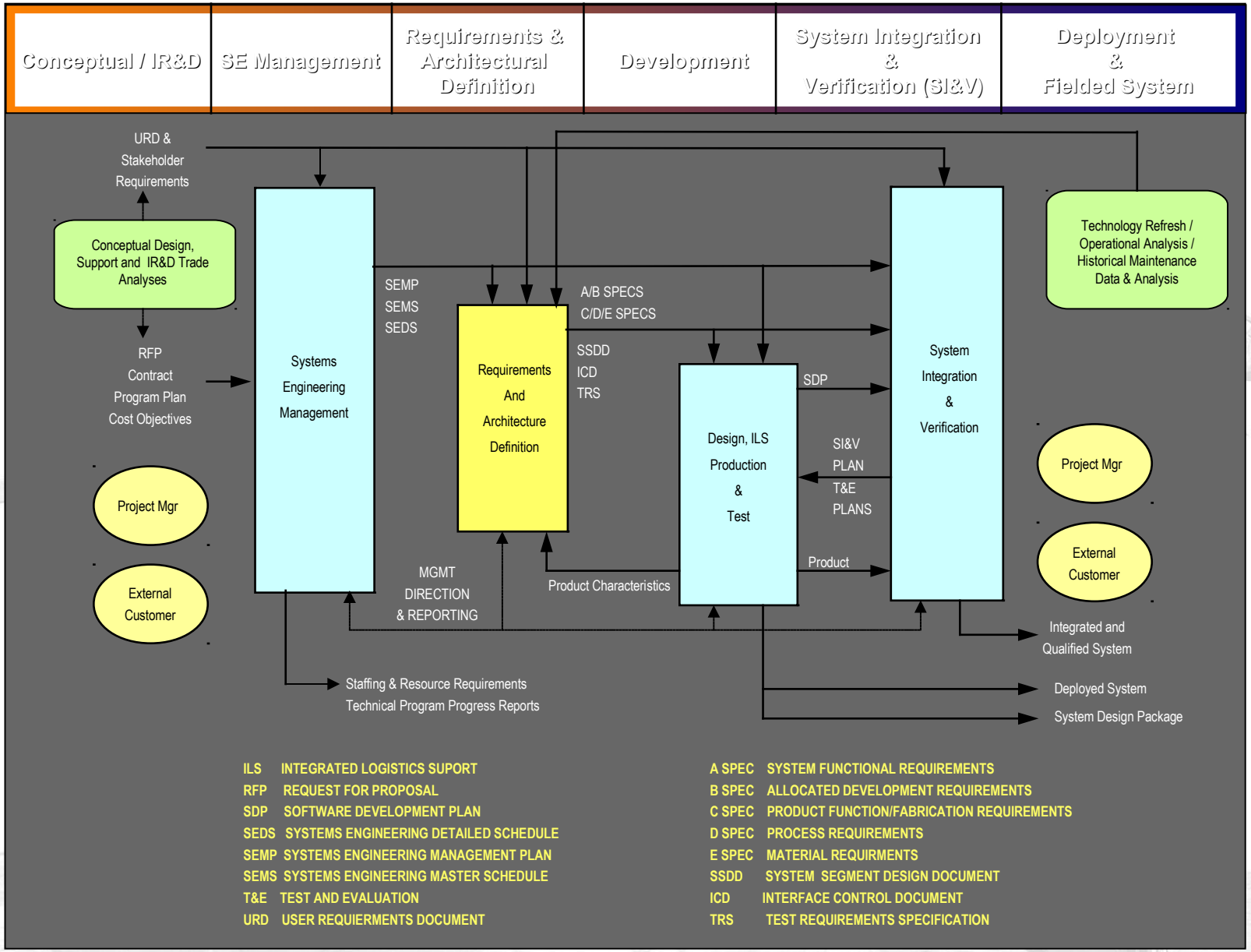
Our Company

28 YEARS of TECHNICAL SERVICE

A Systems Engineering Approach to *Integrated* Diagnostics and Prognostics

- Requirements Derivation
- Requirements Flow down
- Design Development
- Design Optimization
- Embedded Systems
- Life Cycle Support

eXpress



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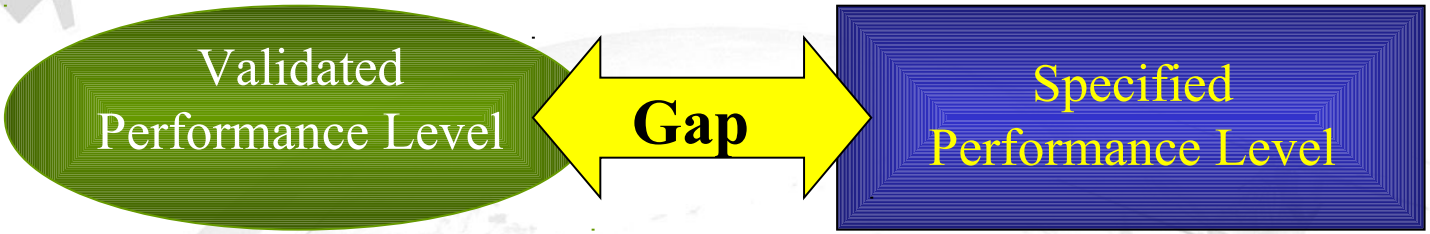
Performance Risk Defined



Performance Risk is

- ***Uncertainty*** in the ability of a design to meet the specified performance level *and* the ***consequences*** thereof
- The gap between the validated and specified performance levels and the consequences of that gap

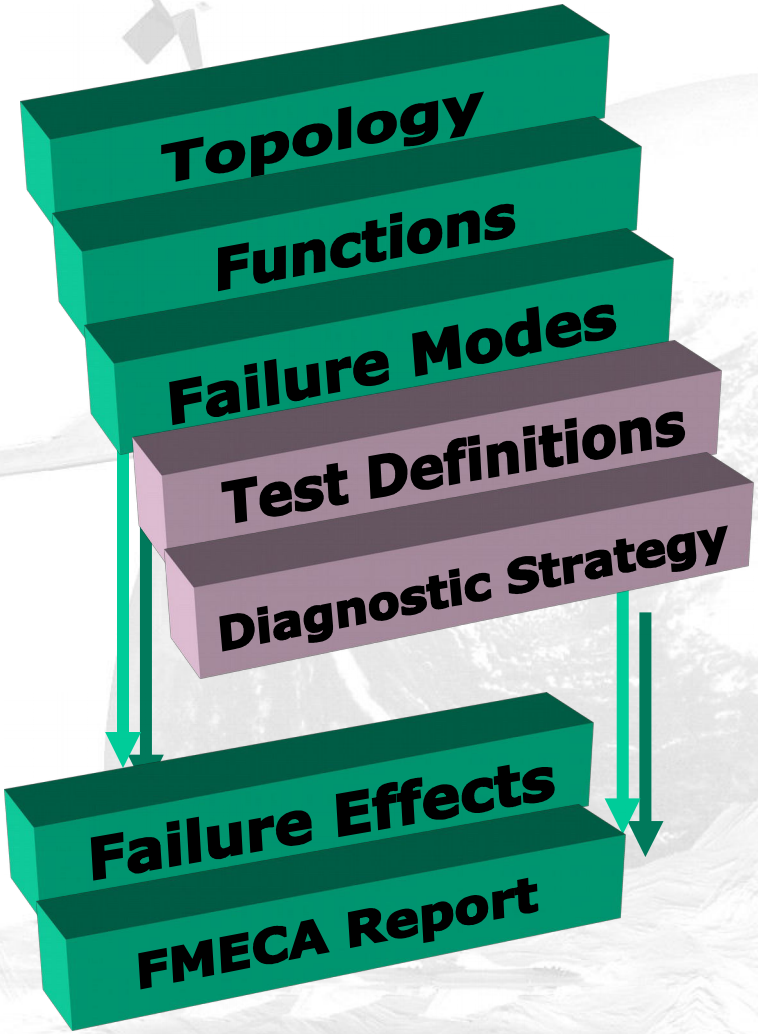
"Performance" is defined broadly to include

- Operability, Functionality, **Safety**, Testability, Affordability, Reliability, Availability, Maintainability, *etc*.
- Any dimension of value to the customer

Today's Technology Provides Process Improvement To *Fill the Gap*

- **Enhanced Diagnostics Modeling Provides:**
  - Improved Fault Detection Confidence (FD%)
  - Improved Fault Isolation to Optimum Repair Level (FI%)
  - Reduced False Alarms / False Removals (FA%)
  - Lower Mean Time to Isolate (MTTI)
  - Improved Operational Availability (Ao)
  - Improved Safety Through Critical Fault Analysis (FMECA)
  - Reduced Life Cycle Cost

Development Information Model

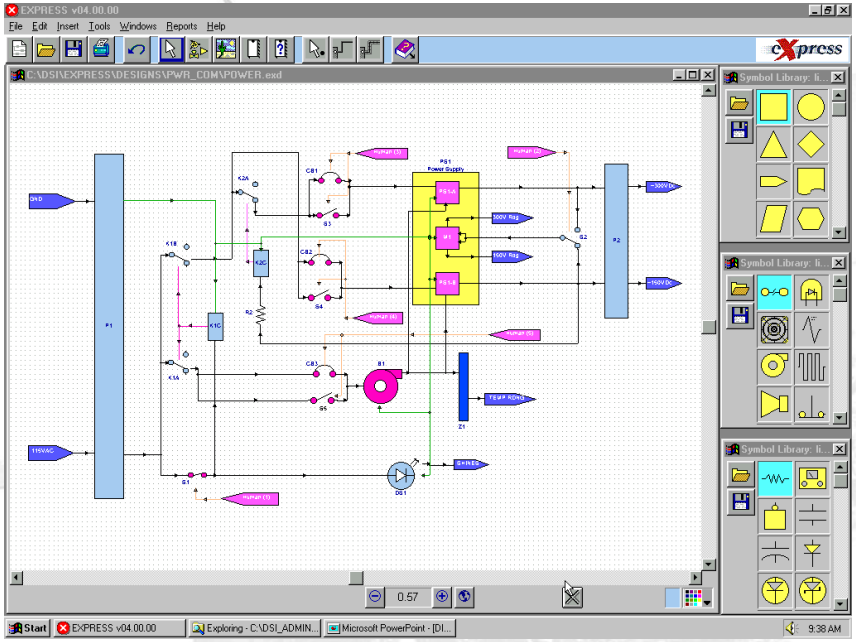


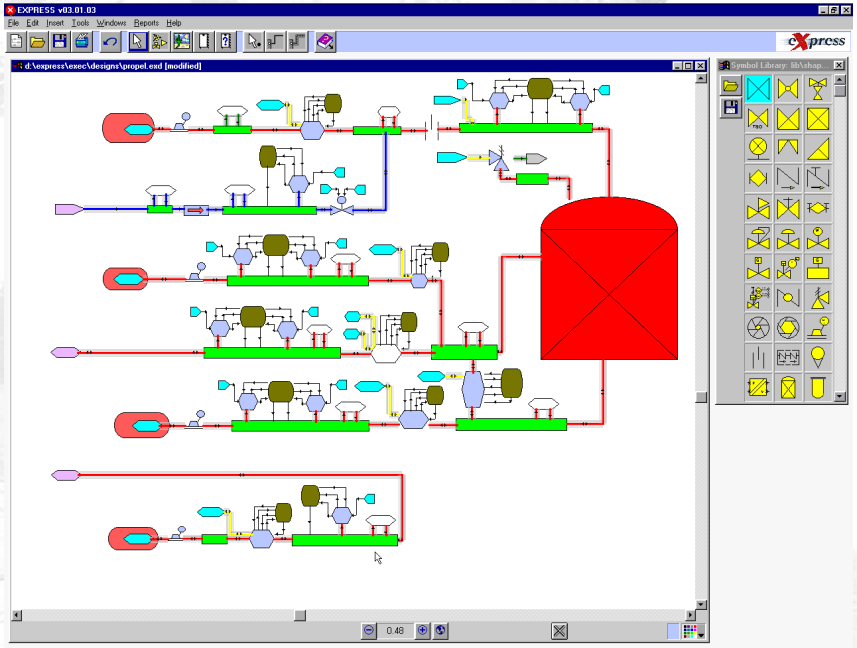
- Topology (Visualization)
- Functions (Objects + Nets)
- Failure Modes (FMECA)
- Test Definitions (Testing)
- Diagnostic Strategy
- Failure Effects (FMECA)
- FMECA Report
  - Working on DMECA

    (Degraded Mode Effect and Criticality Analysis)

Global Modeling

- Electrical
- Electronic
- Mechanical
- Hydraulic
- Optical
- Software
- Process





- Fully Hierarchical
- Object-Oriented
- Networked

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Diagnostic Outputs

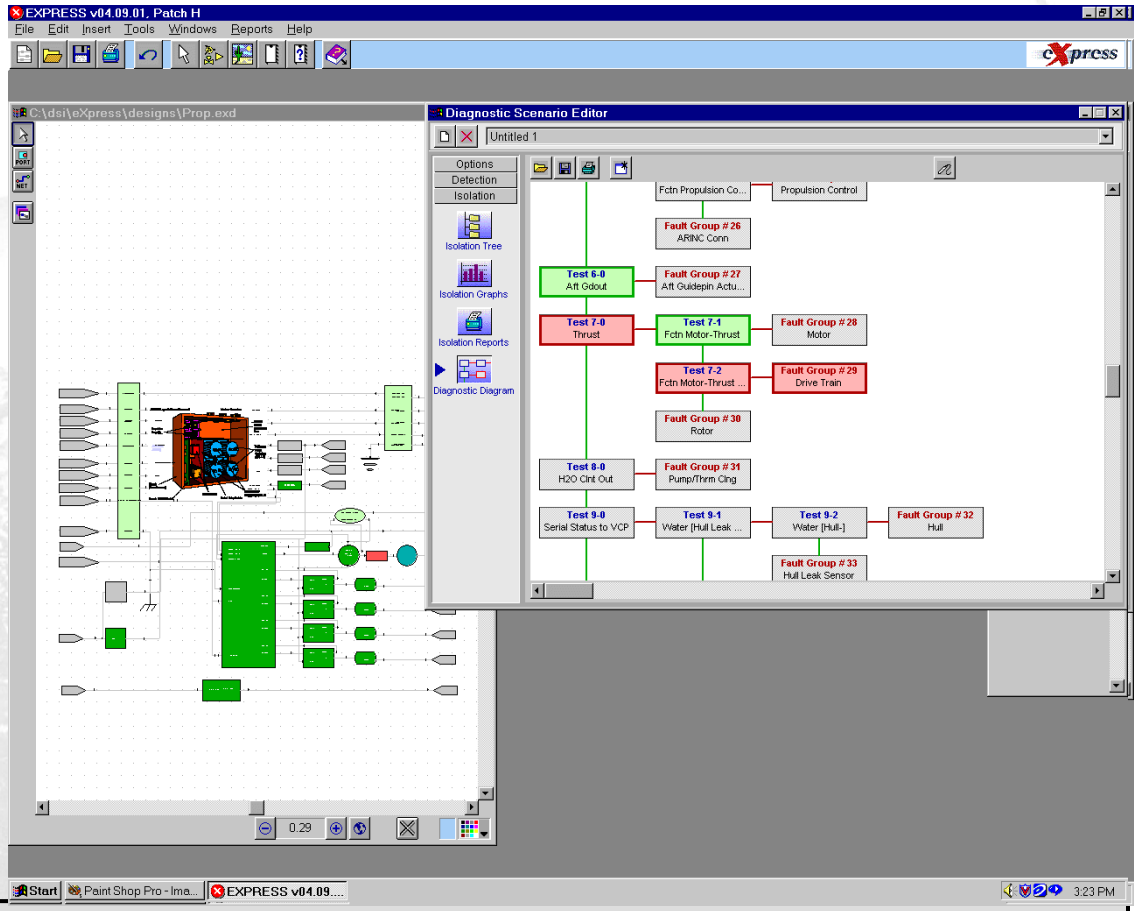
Diagnostic Fault Tree

Provides an interactive interface to “exercise” the diagnostics.

Provides means to “check” models for validity.

Quickly Identifies problem areas (i.e.. Large fault / ambiguity groups)

Can be used for Intelligent troubleshooting



- Light Green - partially proven good - not yet suspected
- Green- proven good
- Light Blue Stimuli necessary for test
- Yellow - suspected, in current suspect set
- Teal - secondary suspects, not in the current suspects set but could be responsible for a previously performed test that failed
- Dark Red - contains potentially failed components, in AG
- Light Red - higher level part for which a lower level part is color dark red
- Dark Blue -I/O Test Point

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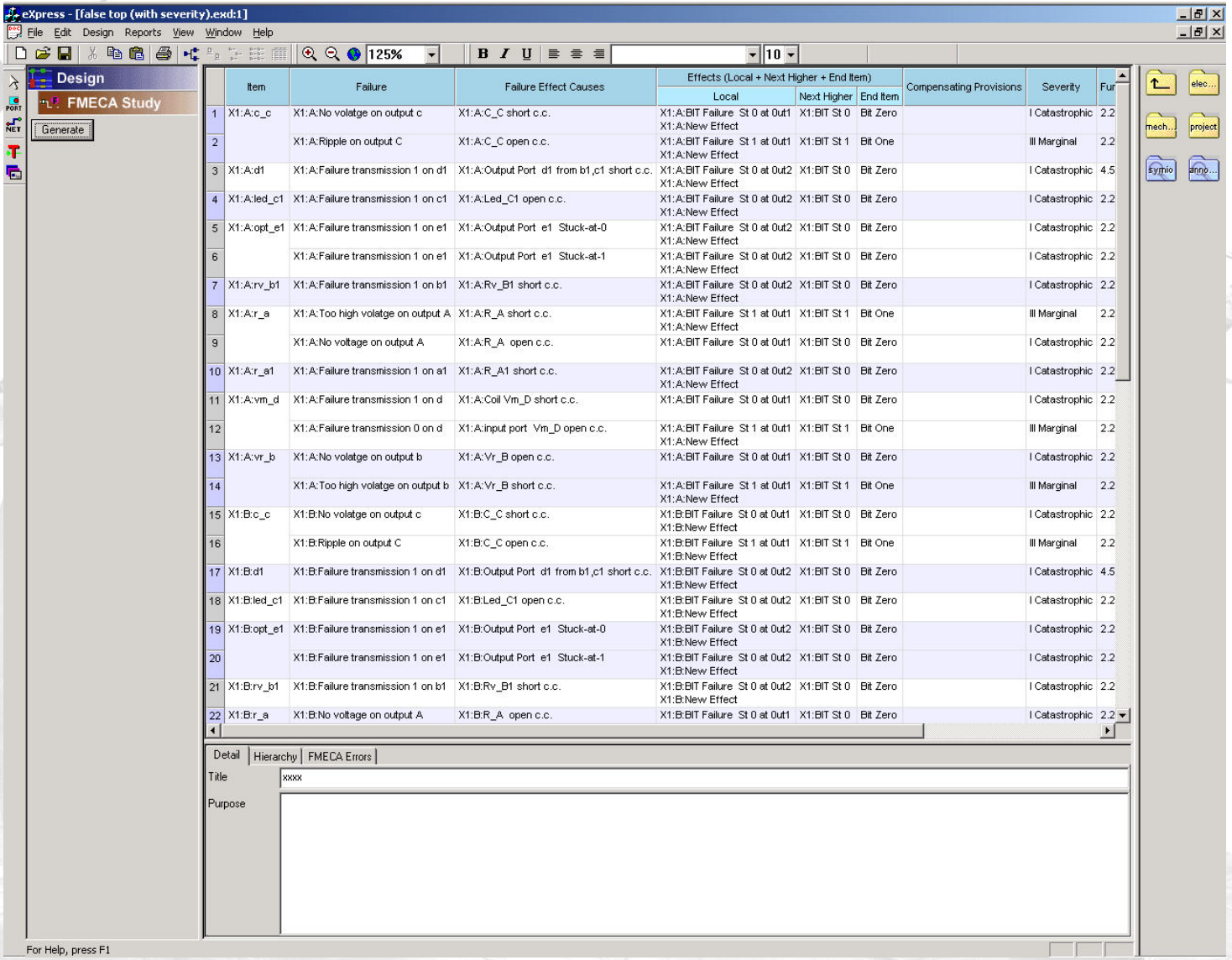
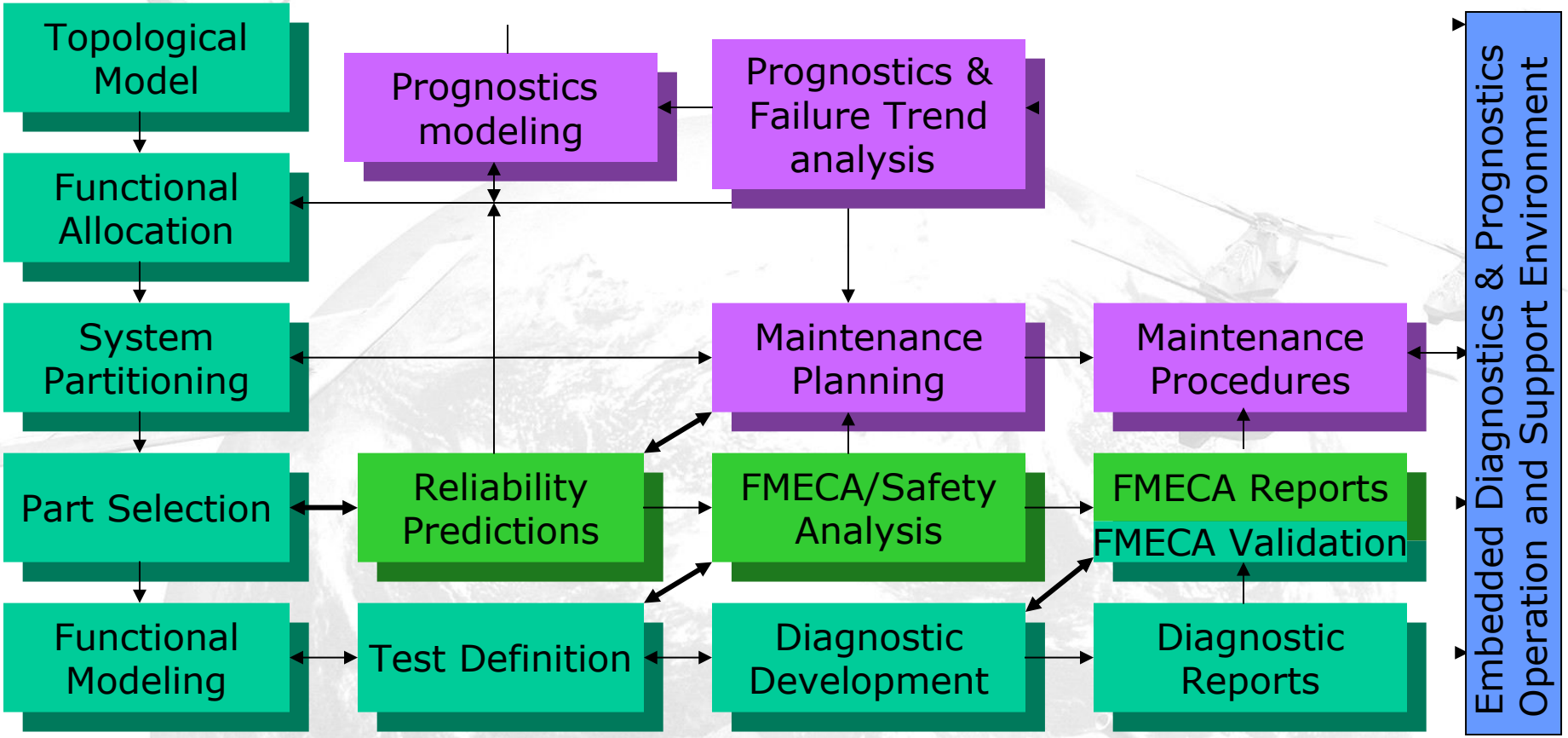
FMECA Output



	Item	Failure	Failure Effect Causes	Effects (Local + Next Higher + End Item)			Compensating Provisions	Severity	Fur
				Local	Next Higher	End Item			
1	X1:A:c_c	X1:A:No volatge on output c	X1:A:C_C short c.c.	X1:A:BIT Failure St 0 at 0ut1 X1:A:New Effect	X1:BIT St 0	Bit Zero		I Catastrophic	2.2
2		X1:A:Ripple on output C	X1:A:C_C open c.c.	X1:A:BIT Failure St 1 at 0ut1 X1:A:New Effect	X1:BIT St 1	Bit One		III Marginal	2.2
3	X1:A:d1	X1:A:Failure transmission 1 on d1	X1:A:Output Port d1 from b1,c1 short c.c.	X1:A:BIT Failure St 0 at 0ut2 X1:A:New Effect	X1:BIT St 0	Bit Zero		I Catastrophic	4.5
4	X1:A:led_c1	X1:A:Failure transmission 1 on c1	X1:A:Led_C1 open c.c.	X1:A:BIT Failure St 0 at 0ut2 X1:A:New Effect	X1:BIT St 0	Bit Zero		I Catastrophic	2.2
5	X1:A:opt_e1	X1:A:Failure transmission 1 on e1	X1:A:Output Port e1 Stuck-at-0	X1:A:BIT Failure St 0 at 0ut2 X1:A:New Effect	X1:BIT St 0	Bit Zero		I Catastrophic	2.2
6		X1:A:Failure transmission 1 on e1	X1:A:Output Port e1 Stuck-at-1	X1:A:BIT Failure St 0 at 0ut2 X1:A:New Effect	X1:BIT St 0	Bit Zero		I Catastrophic	2.2
7	X1:A:rv_b1	X1:A:Failure transmission 1 on b1	X1:A:Rv_B1 short c.c.	X1:A:BIT Failure St 0 at 0ut2 X1:A:New Effect	X1:BIT St 0	Bit Zero		I Catastrophic	2.2
8	X1:A:r_a	X1:A:Too high volatge on output A	X1:A:R_A short c.c.	X1:A:BIT Failure St 1 at 0ut1 X1:A:New Effect	X1:BIT St 1	Bit One		III Marginal	2.2
9		X1:A:No voltage on output A	X1:A:R_A open c.c.	X1:A:BIT Failure St 0 at 0ut1	X1:BIT St 0	Bit Zero		I Catastrophic	2.2
10	X1:A:r_a1	X1:A:Failure transmission 1 on a1	X1:A:R_A1 short c.c.	X1:A:BIT Failure St 0 at 0ut2 X1:A:New Effect	X1:BIT St 0	Bit Zero		I Catastrophic	2.2
11	X1:A:vm_d	X1:A:Failure transmission 1 on d	X1:A:Coil Vm_D short c.c.	X1:A:BIT Failure St 0 at 0ut1	X1:BIT St 0	Bit Zero		I Catastrophic	2.2
12		X1:A:Failure transmission 0 on d	X1:A:input port Vm_D open c.c.	X1:A:BIT Failure St 1 at 0ut1 X1:A:New Effect	X1:BIT St 1	Bit One		III Marginal	2.2
13	X1:A:vr_b	X1:A:No volatge on output b	X1:A:Vr_B open c.c.	X1:A:BIT Failure St 0 at 0ut1	X1:BIT St 0	Bit Zero		I Catastrophic	2.2
14		X1:A:Too high volatge on output b	X1:A:Vr_B short c.c.	X1:A:BIT Failure St 1 at 0ut1 X1:A:New Effect	X1:BIT St 1	Bit One		III Marginal	2.2
15	X1:B:c_c	X1:B:No volatge on output c	X1:B:C_C short c.c.	X1:B:BIT Failure St 0 at 0ut1 X1:B:New Effect	X1:BIT St 0	Bit Zero		I Catastrophic	2.2
16		X1:B:Ripple on output C	X1:B:C_C open c.c.	X1:B:BIT Failure St 1 at 0ut1 X1:B:New Effect	X1:BIT St 1	Bit One		III Marginal	2.2
17	X1:B:d1	X1:B:Failure transmission 1 on d1	X1:B:Output Port d1 from b1,c1 short c.c.	X1:B:BIT Failure St 0 at 0ut2 X1:B:New Effect	X1:BIT St 0	Bit Zero		I Catastrophic	4.5
18	X1:B:led_c1	X1:B:Failure transmission 1 on c1	X1:B:Led_C1 open c.c.	X1:B:BIT Failure St 0 at 0ut2 X1:B:New Effect	X1:BIT St 0	Bit Zero		I Catastrophic	2.2
19	X1:B:opt_e1	X1:B:Failure transmission 1 on e1	X1:B:Output Port e1 Stuck-at-0	X1:B:BIT Failure St 0 at 0ut2 X1:B:New Effect	X1:BIT St 0	Bit Zero		I Catastrophic	2.2
20		X1:B:Failure transmission 1 on e1	X1:B:Output Port e1 Stuck-at-1	X1:B:BIT Failure St 0 at 0ut2 X1:B:New Effect	X1:BIT St 0	Bit Zero		I Catastrophic	2.2
21	X1:B:rv_b1	X1:B:Failure transmission 1 on b1	X1:B:Rv_B1 short c.c.	X1:B:BIT Failure St 0 at 0ut2 X1:B:New Effect	X1:BIT St 0	Bit Zero		I Catastrophic	2.2
22	X1:B:r_a	X1:B:No voltage on output A	X1:B:R_A open c.c.	X1:B:BIT Failure St 0 at 0ut1	X1:BIT St 0	Bit Zero		I Catastrophic	2.2

Process Interoperability



Testability / Diagnosability | **Testability Updates**

Reliability / Safety | **Reliability Updates**

Maintainability | **Maintainability Updates**

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Typical Model Types Developed or Supported

- Reliability
  - Provides Data to Diagnostics Models

- Functional
- Dependency
- Failure Mode

→ Design Direction
→ Design Assessment
→ Design Optimization
→ Support to Ground Operations

- Rule Base
- Case Base
- Model Based Reasoner (MBR)
- AI
- Prognostic

→ Higher Order Run Time

→ Require Developed System

→ Derive Information from Functional, Dependency and Failure Information

→ Support to Optimization Studies

Systems Process at Work

- RAH-66 Comanche Program
- Boeing-Sikorsky-US Army

Diagnostic Design Requirements Analysis Guide (DDRAG)

Note: Document contents are export restricted with distribution limited to US Government agencies

For Distribution and questions, please contact:

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Systems Process at Work

DDRAG Purpose

- Comanche Team Desktop Reference
  - Ensures Standard Processes and Procedures for All Levels of Diagnostics Design Development
- Identifies Processes Needed to Define Diagnostics Design Requirements
  - Equipment
  - Subsystems
  - System / Segment
  - Air Vehicle
  - External Diagnostics
- Defines Operational Flight Program and Off-Board Diagnostics Requirements

Design Process management

- All Levels of Design Data and Tools Need to be Interoperable
- Tools Need to Support Open Information Architecture
- Process Needs to be Managed Through an Integrated Product Development Environment (IPDE)
  - A Concept Development System was Developed for NASA on the 2nd Gen RLV / SLI Project to Meet the Interoperability Needs
    - IVHM Systems Management Environment (ISME)
      - **Data Management**
      - **Translation between Tools, Data and ISME**
      - **Version / Configuration Control**
      - **Audit Trail Management**
      - **User Control**
      - **Security**

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Important Enterprise Features