Implementing ISDD as Design-to-Test (DTT)

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What's in it for me (WIIFM)?

- **Why can't I implement diagnostic analyses at my place of work? (Why won't they listen to me?)**
  - **The value-added benefit is not clear**
- **What is the difference between System Engineering and Test Engineering?**
  - **They are the same thing—from different viewpoints**
- **What is Design-to-Test, and why should I try to use that approach, when it's not my department's responsibility?**
  - **Because it enhances productivity capabilities**
  - **Because it integrates the efforts of all teams**
  - **Because it can be a competitive advantage**

Topic Contents

- **Background**
  - **Systems Engineering Concepts**
  - **Integrated Systems Diagnostic Design Environment**
- **From Legacy to Integrated Diagnostics**
  - **Capturing legacy data**
  - **Diagnostic analysis with eXpress**
  - **Moving beyond analysis**
  - **Interconnecting with other process entities**
- **Towards Design-to-Test (DTT) Methodology**
- **Wrapping it up**

Background

Traditional Product Development

Hardware Engineering

System Engineering

Software Engineering

Test Engineering

Life Cycle Engineering

Factory Support Engineering

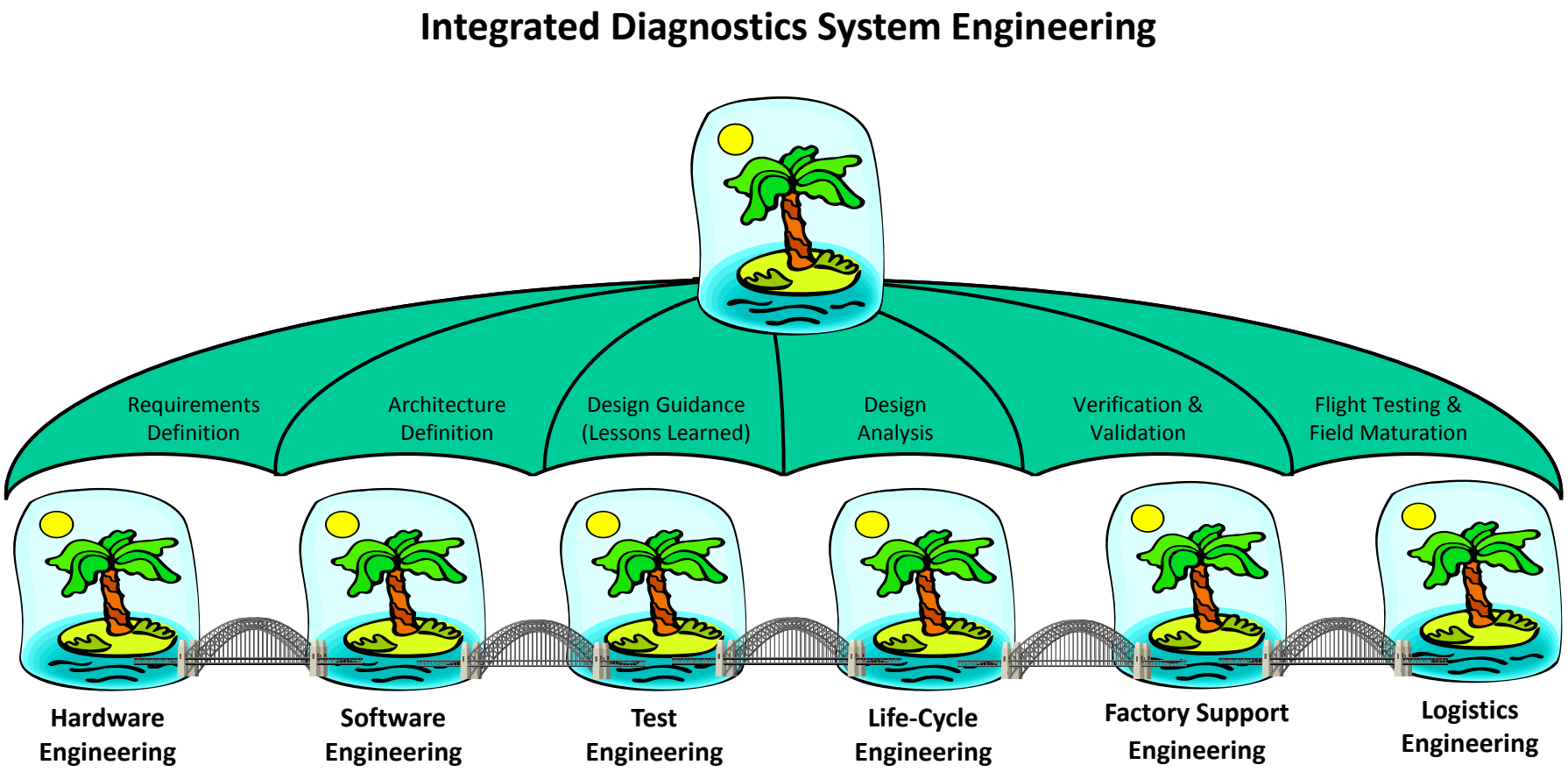
Supplier Management

Logistics Engineering

Diagnostic products are distributed across many IPTs, skill families, business units, and suppliers.

Many historical problems were due to poorly specified or poorly integrated products, and inconsistent or inefficient processes. This can occur even when the individual products meet their own local requirements.

Integrated Diagnostics Process Needed



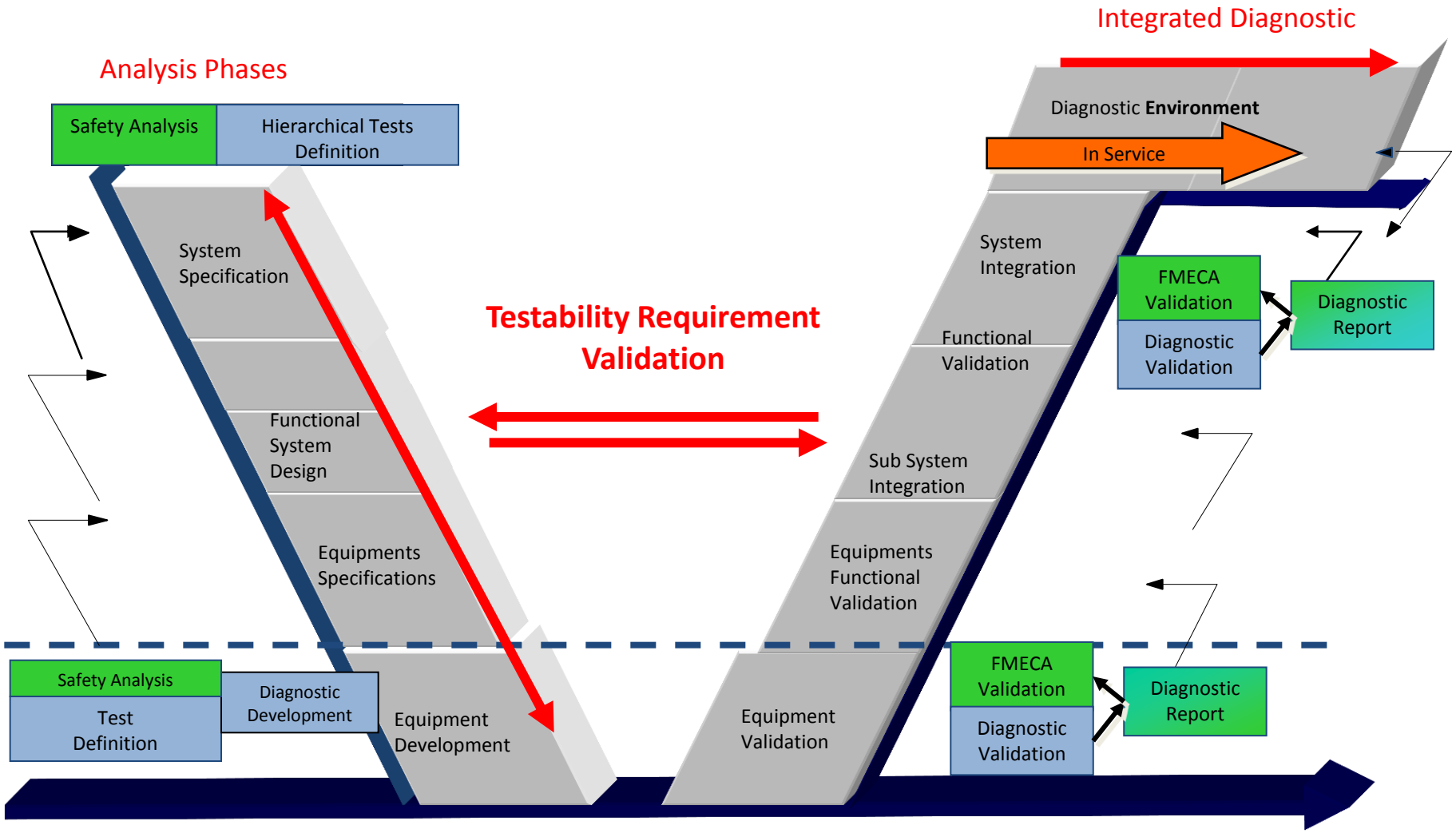
Sustainment Activities

- **Systems Engineering**
  - **Design Activities**
- **Test Engineering**
  - **Verification and Validation Activities**
- **Maintenance Engineering**
  - **Repair Activities**
- **Support Engineering**
  - **Sustainment Activities**
- **Integrated Logistic Systems**
  - **Broad-based Support Activities**

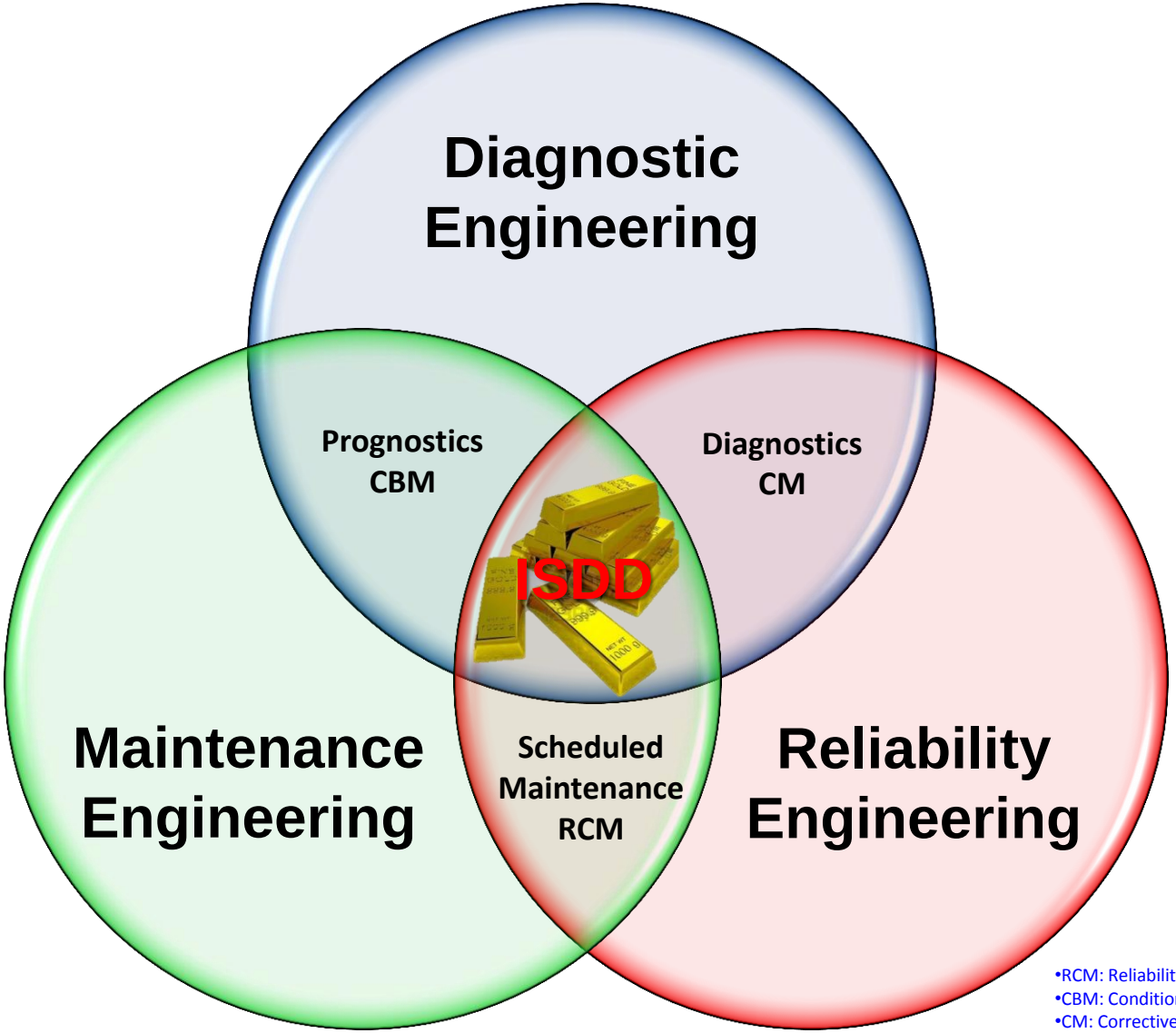
Typical References and Standards

- **Defined in MIL-STD-1814**
  - **The *Integrated Diagnostics* (ID) process is a structured process that maximizes the effectiveness of diagnostics by integrating pertinent elements, such as testability, automatic and manual testing, training, maintenance aiding, and technical information, as a means for providing a cost effective capability to detect and isolate unambiguously all faults known or expected to occur in weapon systems and equipment in order to satisfy weapon system mission requirements.**
- **MIL-HDBK-2165A – Testability**
- **IEEE Std 1522 – Testability and Diagnosability**
- **MIL-STD-1629A – FMECA Procedures**

Systems Engineering Vision

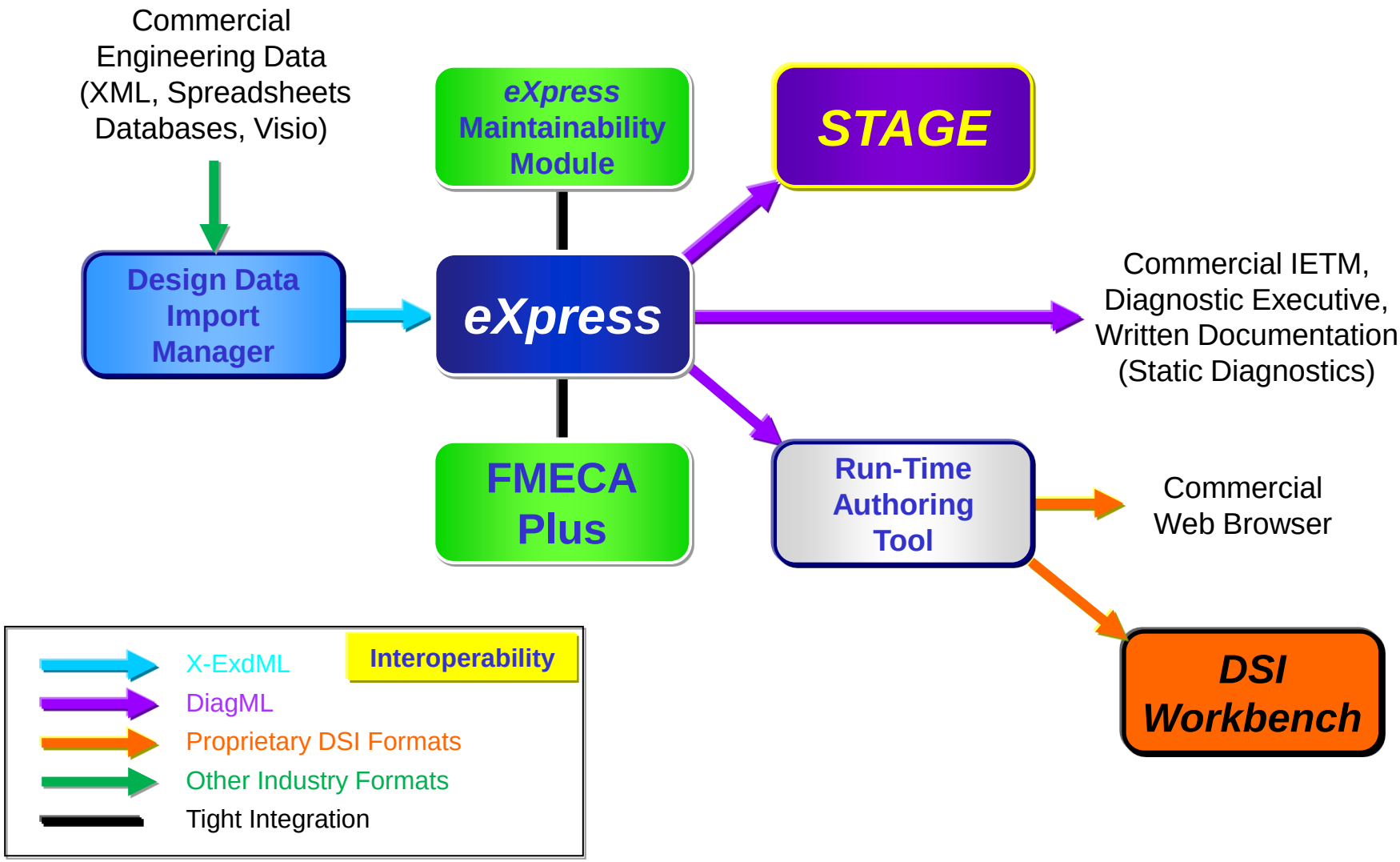


Intersecting Engineering Environments



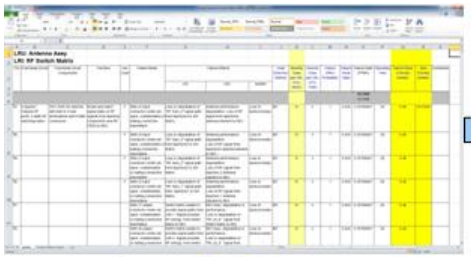
- RCM: Reliability-Centered Maintenance
- CBM: Condition-Based Maintenance
- CM: Corrective Maintenance

The ISDD Vision and Tool Suite



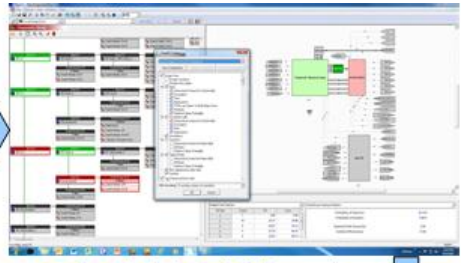
From Legacy to Integrated Diagnostics

Preserving Legacy Designs



Legacy Data Source

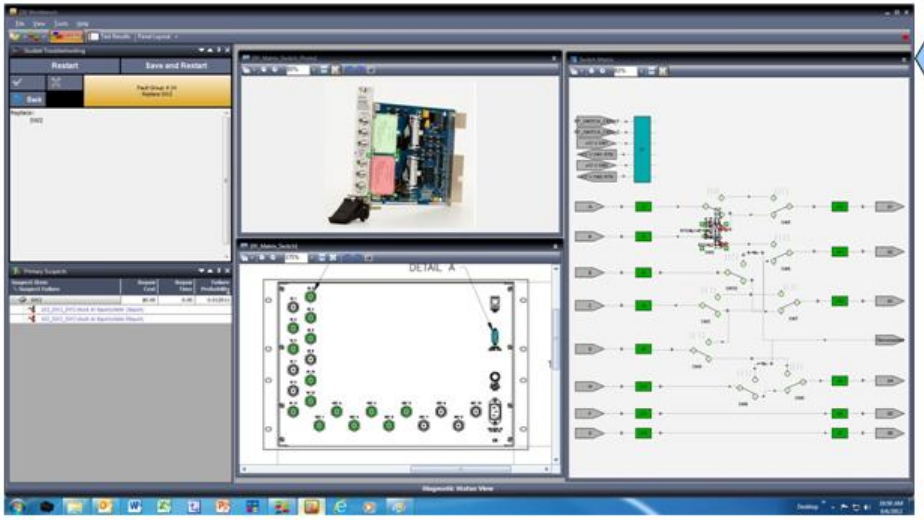
Modified for Tool Import



Analysis Tool & Export

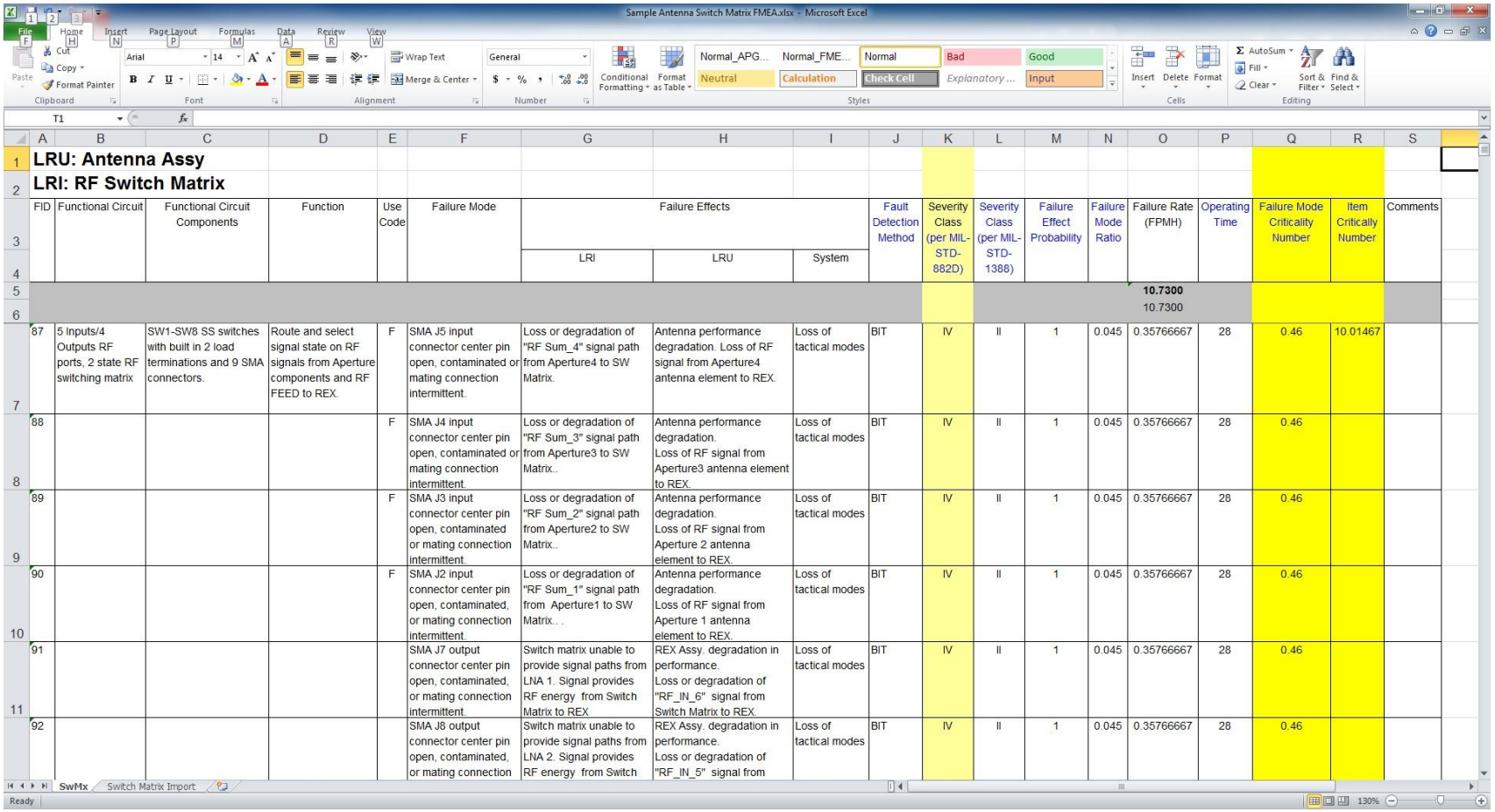
Gathering & Merging
Resources to Analyses

Target Tools:
DSI Workbench &
Test Executive of Choice



Browser Display via Java
Applet for Team Review

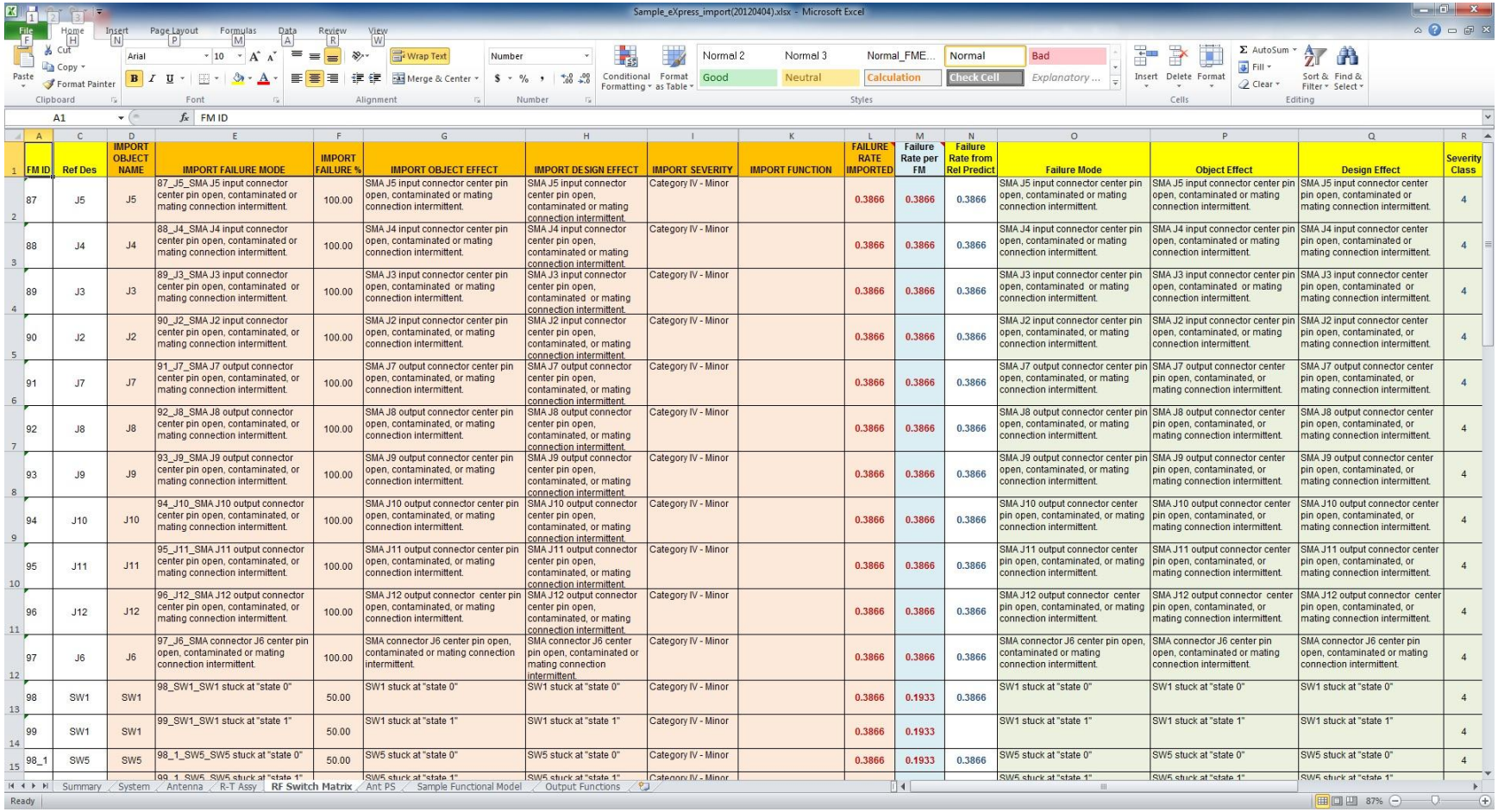
Collecting Legacy Data



FID	Functional Circuit	Functional Circuit Components	Function	Use Code	Failure Mode	Failure Effects: LRI	Failure Effects: LRU	Failure Effects: System	Fault Detection Method	Severity Class (per MIL-STD-882D)	Severity Class (per MIL-STD-1388)	Failure Effect Probability	Failure Mode Ratio	Failure Rate (FPMH)	Operating Time	Failure Mode Criticality Number	Item Criticality Number	Comments
														10.7300				
														10.7300				
87	5 Inputs/4 Outputs RF ports, 2 state RF switching matrix	SW1-SW8 SS switches with built in 2 load terminations and 9 SMA connectors.	Route and select signal state on RF signals from Aperture components and RF FEED to REX.	F	SMA J5 input connector center pin open, contaminated or mating connection intermittent.	Loss or degradation of "RF Sum_4" signal path from Aperture4 to SW Matrix.	Antenna performance degradation. Loss of RF signal from Aperture4 antenna element to REX.	Loss of tactical modes	BIT	IV	II	1	0.045	0.35766667	28	0.46	10.01467	
88				F	SMA J4 input connector center pin open, contaminated or mating connection intermittent.	Loss or degradation of "RF Sum_3" signal path from Aperture3 to SW Matrix..	Antenna performance degradation. Loss of RF signal from Aperture3 antenna element to REX.	Loss of tactical modes	BIT	IV	II	1	0.045	0.35766667	28	0.46		
89				F	SMA J3 input connector center pin open, contaminated or mating connection intermittent.	Loss or degradation of "RF Sum_2" signal path from Aperture2 to SW Matrix..	Antenna performance degradation. Loss of RF signal from Aperture 2 antenna element to REX.	Loss of tactical modes	BIT	IV	II	1	0.045	0.35766667	28	0.46		
90				F	SMA J2 input connector center pin open, contaminated, or mating connection intermittent.	Loss or degradation of "RF Sum_1" signal path from Aperture1 to SW Matrix.. .	Antenna performance degradation. Loss of RF signal from Aperture 1 antenna element to REX.	Loss of tactical modes	BIT	IV	II	1	0.045	0.35766667	28	0.46		
91					SMA J7 output connector center pin open, contaminated, or mating connection intermittent.	Switch matrix unable to provide signal paths from LNA 1. Signal provides RF energy from Switch Matrix to REX.	REX Assy. degradation in performance. Loss or degradation of "RF_IN_6" signal from Switch Matrix to REX.	Loss of tactical modes	BIT	IV	II	1	0.045	0.35766667	28	0.46		
92					SMA J8 output connector center pin open, contaminated, or mating connection	Switch matrix unable to provide signal paths from LNA 2. Signal provides RF energy from Switch	REX Assy. degradation in performance. Loss or degradation of "RF_IN_5" signal from	Loss of tactical modes	BIT	IV	II	1	0.045	0.35766667	28	0.46		

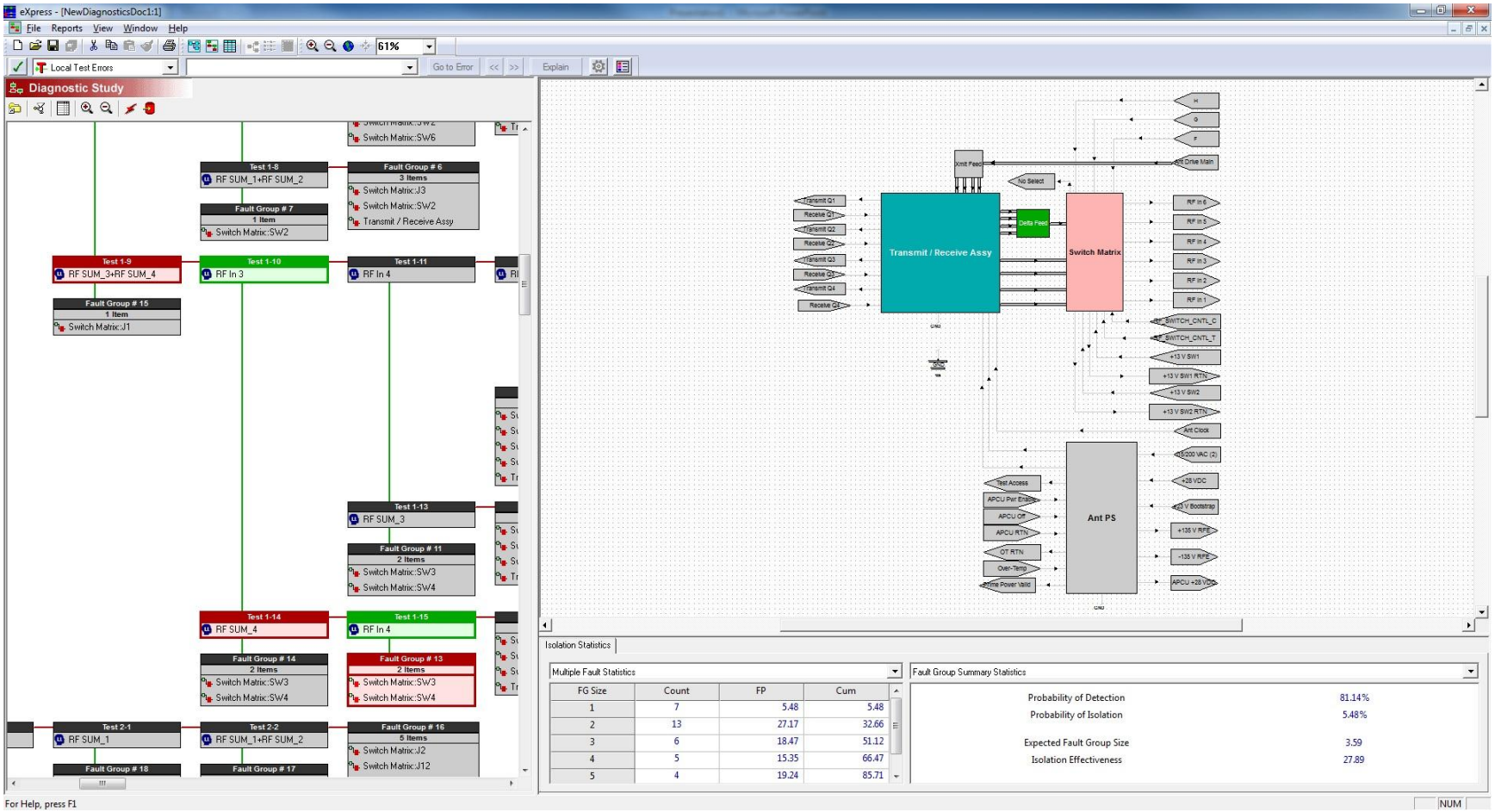
☆ Using existing FMEA/FMECA/ICD, etc.

Preparing for Importing to eXpress

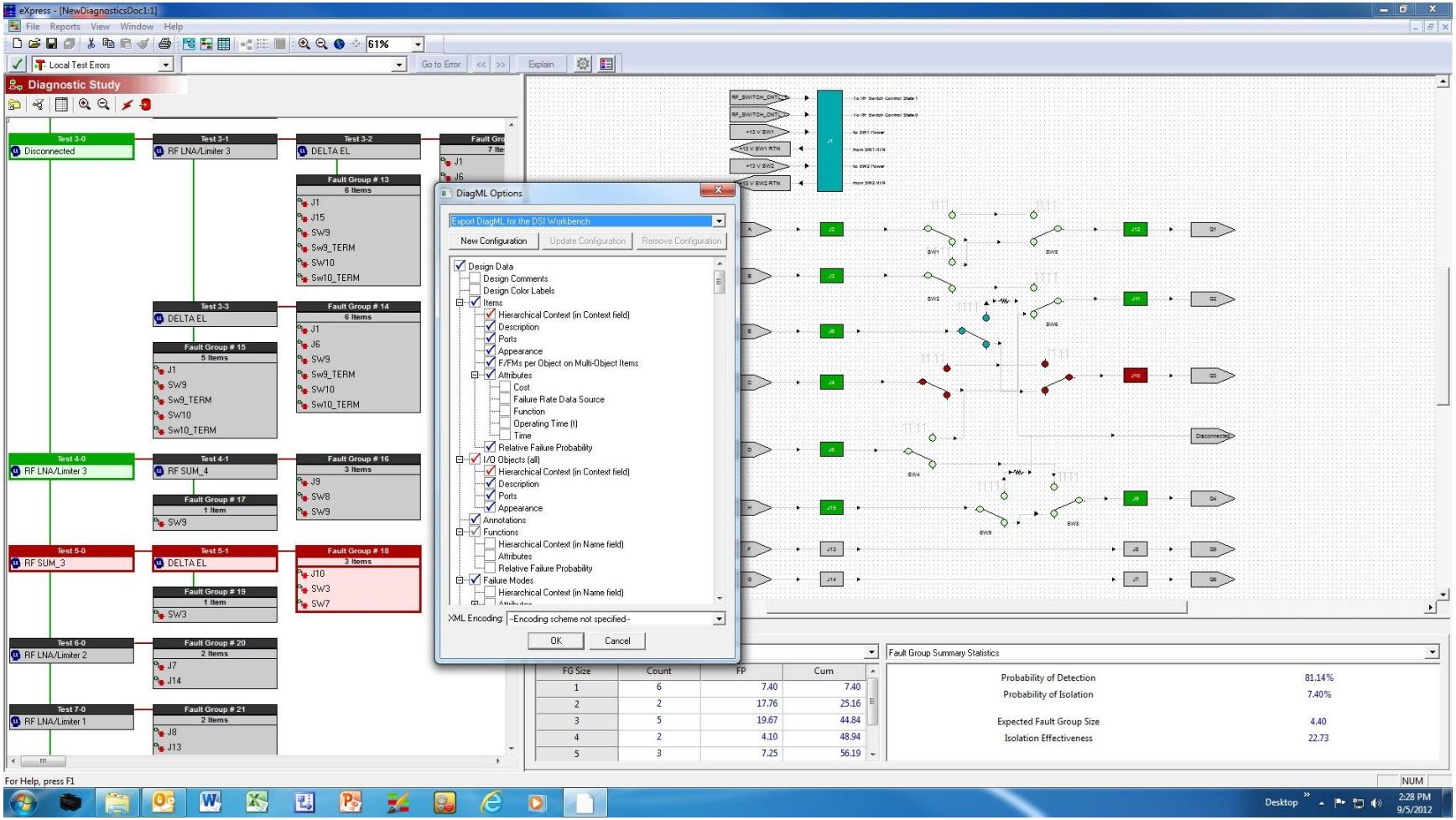


FM ID	Ref Des	IMPORT OBJECT NAME	IMPORT FAILURE MODE	IMPORT FAILURE %	IMPORT OBJECT EFFECT	IMPORT DESIGN EFFECT	IMPORT SEVERITY	IMPORT FUNCTION	FAILURE RATE IMPORTED	Failure Rate per FM	Failure Rate from Rel Predict	Failure Mode	Object Effect	Design Effect	Severity Class
87	J5	J5	87_J5_SMA J5 input connector center pin open, contaminated or mating connection intermittent.	100.00	SMA J5 input connector center pin open, contaminated or mating connection intermittent.	SMA J5 input connector center pin open, contaminated or mating connection intermittent.	Category IV - Minor		0.3866	0.3866	0.3866	SMA J5 input connector center pin open, contaminated or mating connection intermittent.	SMA J5 input connector center pin open, contaminated or mating connection intermittent.	SMA J5 input connector center pin open, contaminated or mating connection intermittent.	4
88	J4	J4	88_J4_SMA J4 input connector center pin open, contaminated or mating connection intermittent.	100.00	SMA J4 input connector center pin open, contaminated or mating connection intermittent.	SMA J4 input connector center pin open, contaminated or mating connection intermittent.	Category IV - Minor		0.3866	0.3866	0.3866	SMA J4 input connector center pin open, contaminated or mating connection intermittent.	SMA J4 input connector center pin open, contaminated or mating connection intermittent.	SMA J4 input connector center pin open, contaminated or mating connection intermittent.	4
89	J3	J3	89_J3_SMA J3 input connector center pin open, contaminated or mating connection intermittent.	100.00	SMA J3 input connector center pin open, contaminated or mating connection intermittent.	SMA J3 input connector center pin open, contaminated or mating connection intermittent.	Category IV - Minor		0.3866	0.3866	0.3866	SMA J3 input connector center pin open, contaminated or mating connection intermittent.	SMA J3 input connector center pin open, contaminated or mating connection intermittent.	SMA J3 input connector center pin open, contaminated or mating connection intermittent.	4
90	J2	J2	90_J2_SMA J2 input connector center pin open, contaminated, or mating connection intermittent.	100.00	SMA J2 input connector center pin open, contaminated, or mating connection intermittent.	SMA J2 input connector center pin open, contaminated, or mating connection intermittent.	Category IV - Minor		0.3866	0.3866	0.3866	SMA J2 input connector center pin open, contaminated, or mating connection intermittent.	SMA J2 input connector center pin open, contaminated, or mating connection intermittent.	SMA J2 input connector center pin open, contaminated, or mating connection intermittent.	4
91	J7	J7	91_J7_SMA J7 output connector center pin open, contaminated, or mating connection intermittent.	100.00	SMA J7 output connector center pin open, contaminated, or mating connection intermittent.	SMA J7 output connector center pin open, contaminated, or mating connection intermittent.	Category IV - Minor		0.3866	0.3866	0.3866	SMA J7 output connector center pin open, contaminated, or mating connection intermittent.	SMA J7 output connector center pin open, contaminated, or mating connection intermittent.	SMA J7 output connector center pin open, contaminated, or mating connection intermittent.	4
92	J8	J8	92_J8_SMA J8 output connector center pin open, contaminated, or mating connection intermittent.	100.00	SMA J8 output connector center pin open, contaminated, or mating connection intermittent.	SMA J8 output connector center pin open, contaminated, or mating connection intermittent.	Category IV - Minor		0.3866	0.3866	0.3866	SMA J8 output connector center pin open, contaminated, or mating connection intermittent.	SMA J8 output connector center pin open, contaminated, or mating connection intermittent.	SMA J8 output connector center pin open, contaminated, or mating connection intermittent.	4
93	J9	J9	93_J9_SMA J9 output connector center pin open, contaminated, or mating connection intermittent.	100.00	SMA J9 output connector center pin open, contaminated, or mating connection intermittent.	SMA J9 output connector center pin open, contaminated, or mating connection intermittent.	Category IV - Minor		0.3866	0.3866	0.3866	SMA J9 output connector center pin open, contaminated, or mating connection intermittent.	SMA J9 output connector center pin open, contaminated, or mating connection intermittent.	SMA J9 output connector center pin open, contaminated, or mating connection intermittent.	4
94	J10	J10	94_J10_SMA J10 output connector center pin open, contaminated, or mating connection intermittent.	100.00	SMA J10 output connector center pin open, contaminated, or mating connection intermittent.	SMA J10 output connector center pin open, contaminated, or mating connection intermittent.	Category IV - Minor		0.3866	0.3866	0.3866	SMA J10 output connector center pin open, contaminated, or mating connection intermittent.	SMA J10 output connector center pin open, contaminated, or mating connection intermittent.	SMA J10 output connector center pin open, contaminated, or mating connection intermittent.	4
95	J11	J11	95_J11_SMA J11 output connector center pin open, contaminated, or mating connection intermittent.	100.00	SMA J11 output connector center pin open, contaminated, or mating connection intermittent.	SMA J11 output connector center pin open, contaminated, or mating connection intermittent.	Category IV - Minor		0.3866	0.3866	0.3866	SMA J11 output connector center pin open, contaminated, or mating connection intermittent.	SMA J11 output connector center pin open, contaminated, or mating connection intermittent.	SMA J11 output connector center pin open, contaminated, or mating connection intermittent.	4
96	J12	J12	96_J12_SMA J12 output connector center pin open, contaminated, or mating connection intermittent.	100.00	SMA J12 output connector center pin open, contaminated, or mating connection intermittent.	SMA J12 output connector center pin open, contaminated, or mating connection intermittent.	Category IV - Minor		0.3866	0.3866	0.3866	SMA J12 output connector center pin open, contaminated, or mating connection intermittent.	SMA J12 output connector center pin open, contaminated, or mating connection intermittent.	SMA J12 output connector center pin open, contaminated, or mating connection intermittent.	4
97	J6	J6	97_J6_SMA connector J6 center pin open, contaminated or mating connection intermittent.	100.00	SMA connector J6 center pin open, contaminated or mating connection intermittent.	SMA connector J6 center pin open, contaminated or mating connection intermittent.	Category IV - Minor		0.3866	0.3866	0.3866	SMA connector J6 center pin open, contaminated or mating connection intermittent.	SMA connector J6 center pin open, contaminated or mating connection intermittent.	SMA connector J6 center pin open, contaminated or mating connection intermittent.	4
98	SW1	SW1	98_SW1_SW1 stuck at "state 0"	50.00	SW1 stuck at "state 0"	SW1 stuck at "state 0"	Category IV - Minor		0.3866	0.1933	0.3866	SW1 stuck at "state 0"	SW1 stuck at "state 0"	SW1 stuck at "state 0"	4
99	SW1	SW1	99_SW1_SW1 stuck at "state 1"	50.00	SW1 stuck at "state 1"	SW1 stuck at "state 1"	Category IV - Minor		0.3866	0.1933		SW1 stuck at "state 1"	SW1 stuck at "state 1"	SW1 stuck at "state 1"	4
98_1	SW5	SW5	98_1_SW5_SW5 stuck at "state 0"	50.00	SW5 stuck at "state 0"	SW5 stuck at "state 0"	Category IV - Minor		0.3866	0.1933	0.3866	SW5 stuck at "state 0"	SW5 stuck at "state 0"	SW5 stuck at "state 0"	4
99_1	SW5	SW5	99_1_SW5_SW5 stuck at "state 1"		SW5 stuck at "state 1"	SW5 stuck at "state 1"	Category IV - Minor					SW5 stuck at "state 1"	SW5 stuck at "state 1"	SW5 stuck at "state 1"	

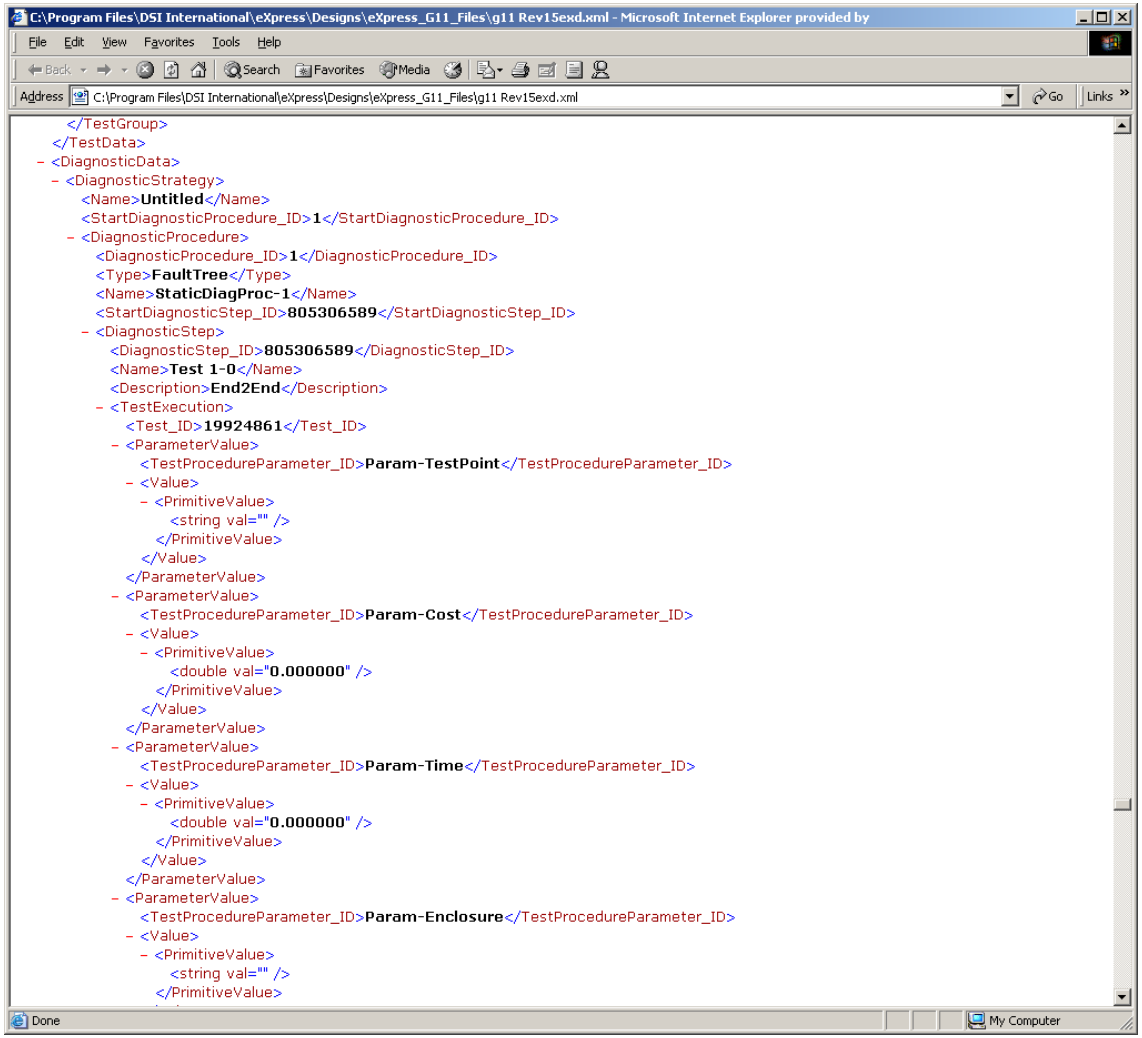
Analyzing at the System Level



Analyzing & Exporting LRU Data



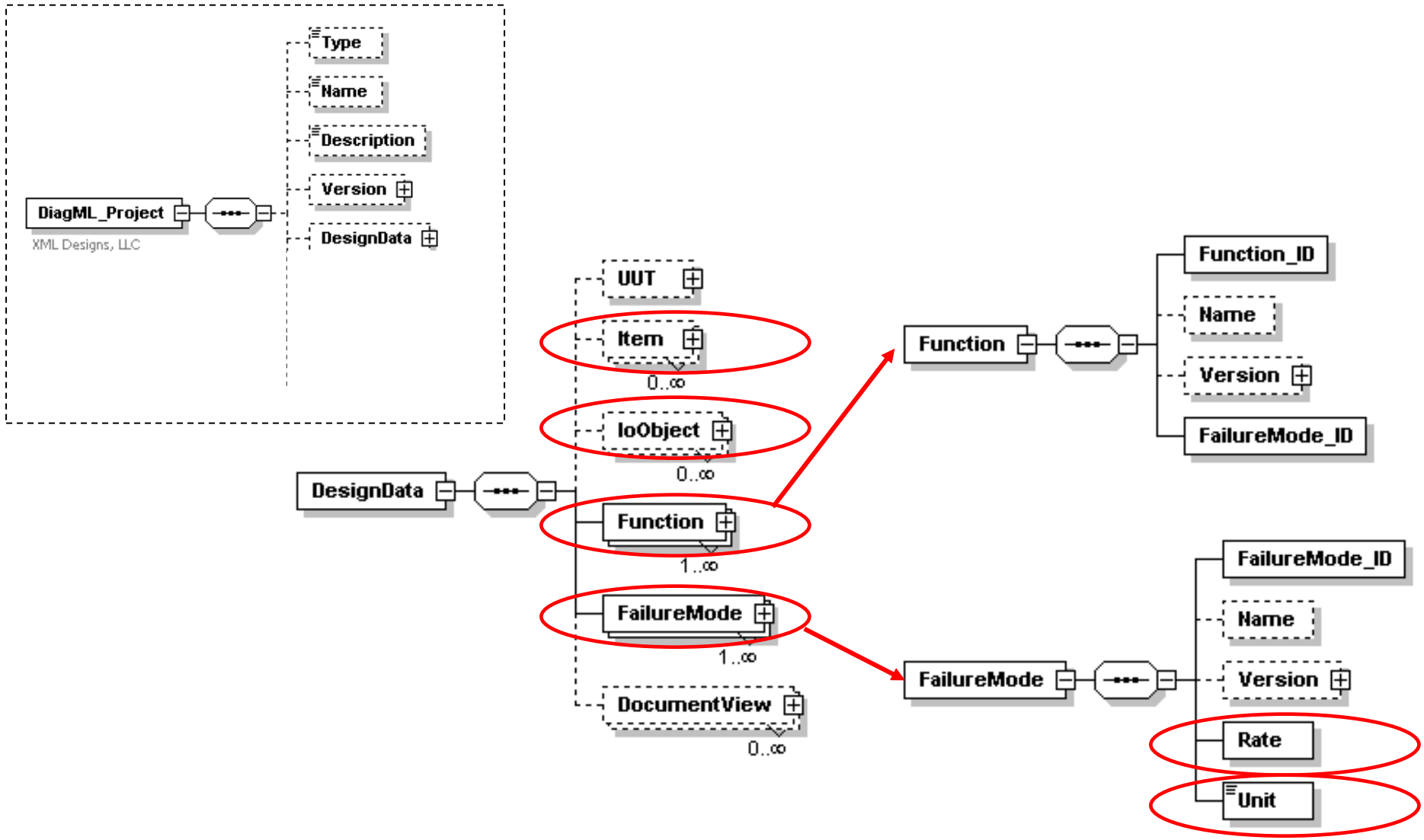
Diag-ML “Test Vector” Export



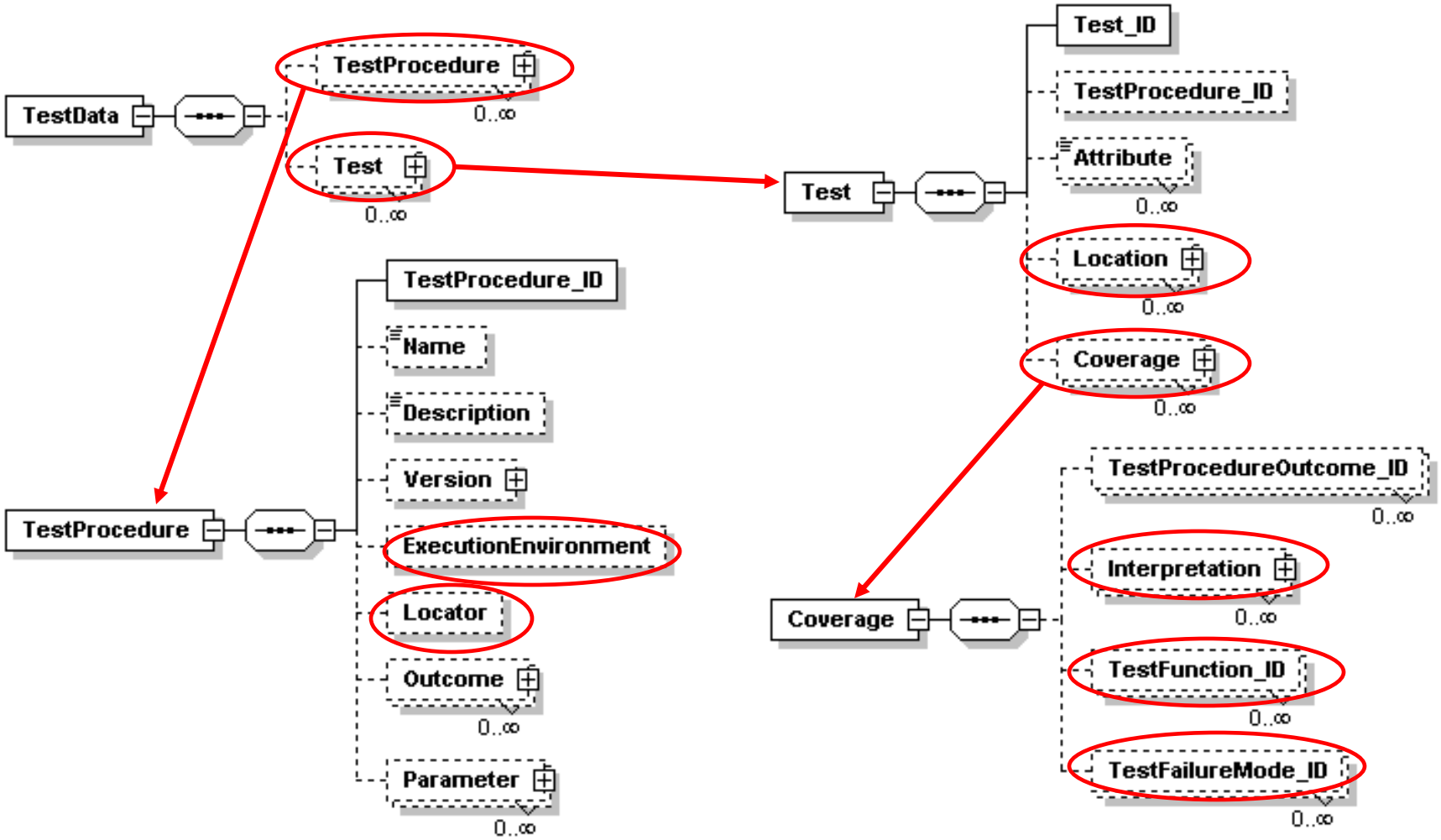
Adding Parameters for Exporting

	Object Abbreviation	Object Type	Item Reference	Failure Prob. Method	Description	Gain	Noise Figure	Reliability (FR) [+]
1	001 T Sw	Component		Default Precedence	T-Switch	0	0	0.00001
2	001A T Sw	Component	001A T Sw	Default Precedence	T-Switch	0	0	0.00001
3	002 T Sw	Component		Default Precedence	T-Switch	0	0	0.00001
4	002A T Sw	Component	002A T Sw	Default Precedence	T-Switch	0	0	0.00001
5	003 T Sw	Component		Default Precedence	T-Switch	0	0	0.00001
6	003A T Sw	Component	003A T Sw	Default Precedence	T-Switch	0	0	0.00001
7	004 T Sw	Component		Default Precedence	T-Switch	0	0	0.00001
8	004A T Sw	Component	004A T Sw	Default Precedence	T-Switch	0	0	0.00001
9	005 T Sw	Component		Default Precedence	T-Switch	0	0	0.00001
10	006 T Sw	Component		Default Precedence	T-Switch	0	0	0.00001
11	007 T Sw	Component		Default Precedence	T-Switch	0	0	0.00001
12	008 T Sw	Component		Default Precedence	T-Switch	0	0	0.00001
13	009 T Sw	Component		Default Precedence	T-Switch	0	0	0.00001
14	010 T Sw	Component		Default Precedence	T-Switch	0	0	0.00001
15	011 T Sw	Component		Default Precedence	T-Switch	0	0	0.00001
16	012 T Sw	Component		Default Precedence	T-Switch	0	0	0.00001
17	1:04	Component		Default Precedence	1:4 Splitter	0	0	0.00001
18	1:04	Component		Default Precedence	1:4 Splitter	0	0	0.00001
19	CMD DF1	Component	CDF1	Default Precedence	Command Despread Fwd	-0.3	0	0.00001
20	OMT1	Component	OMT1	Default Precedence	Square	-0.5	0	0.00001
21	TRF1	Component	TRF1	Default Precedence	TRF June 6 2008 Installed June 7 2006 Removed TA 123	0	0	0.00001
22	TRF2	Component		Default Precedence	TRF	0	0	0.00001
23	GW1 Antenna	Component	GW1	Default Precedence	Antenna	20	0	1
24	<UNNAMED>	Component	CA546K-1	Default Precedence	Coax Attenuator	0	0	1.1
25	<UNNAMED>	Component	CA546K-1	Default Precedence	Coax Attenuator	0	0	1.1
26	<UNNAMED>	Component	CA546K-1	Default Precedence	Coax Attenuator	0	0	1.1
27	<UNNAMED>	Component	CA546K-1	Default Precedence	Coax Attenuator	0	0	1.1
28	<UNNAMED>	Component	CA546K-1	Default Precedence	Coax Attenuator	0	0	1.1
29	<UNNAMED>	Component	CA546K-1	Default Precedence	Coax Attenuator	0	0	1.1
30	<UNNAMED>	Component	CA546K-1	Default Precedence	Coax Attenuator	0	0	1.1
31	<UNNAMED>	Component	CA546K-1	Default Precedence	Coax Attenuator	0	0	1.1
32	BPF1	Component	BPF1	Default Precedence	Band-Pass Filter	-2	0	1.1
33	BPF2	Component	BPF2	Default Precedence	Band-Pass Filter	-2	0	1.1
34	BPF3	Component	BPF3	Default Precedence	Band-Pass Filter	-2	0	1.1
35	BPF4	Component	BPF4	Default Precedence	Band-Pass Filter	-2	0	1.1

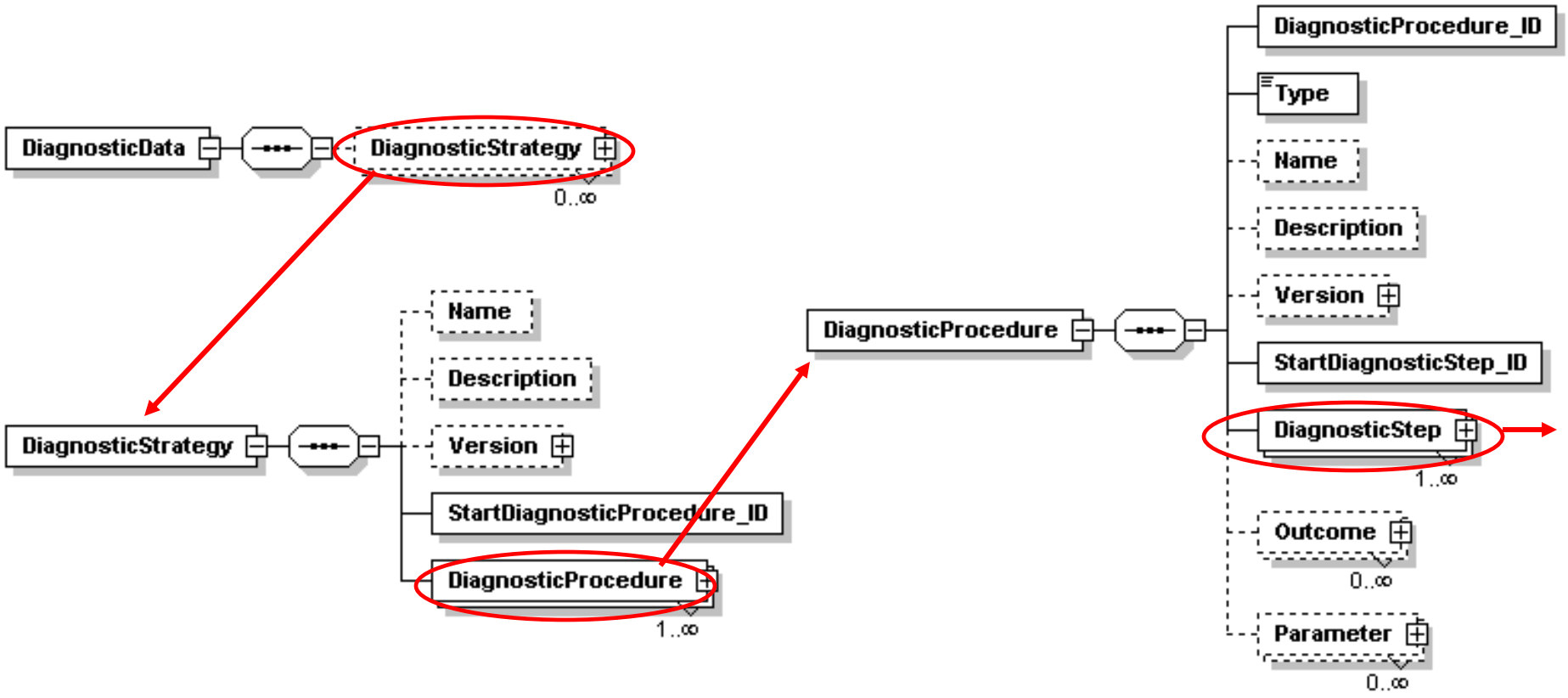
DiagML Implementation (Design)



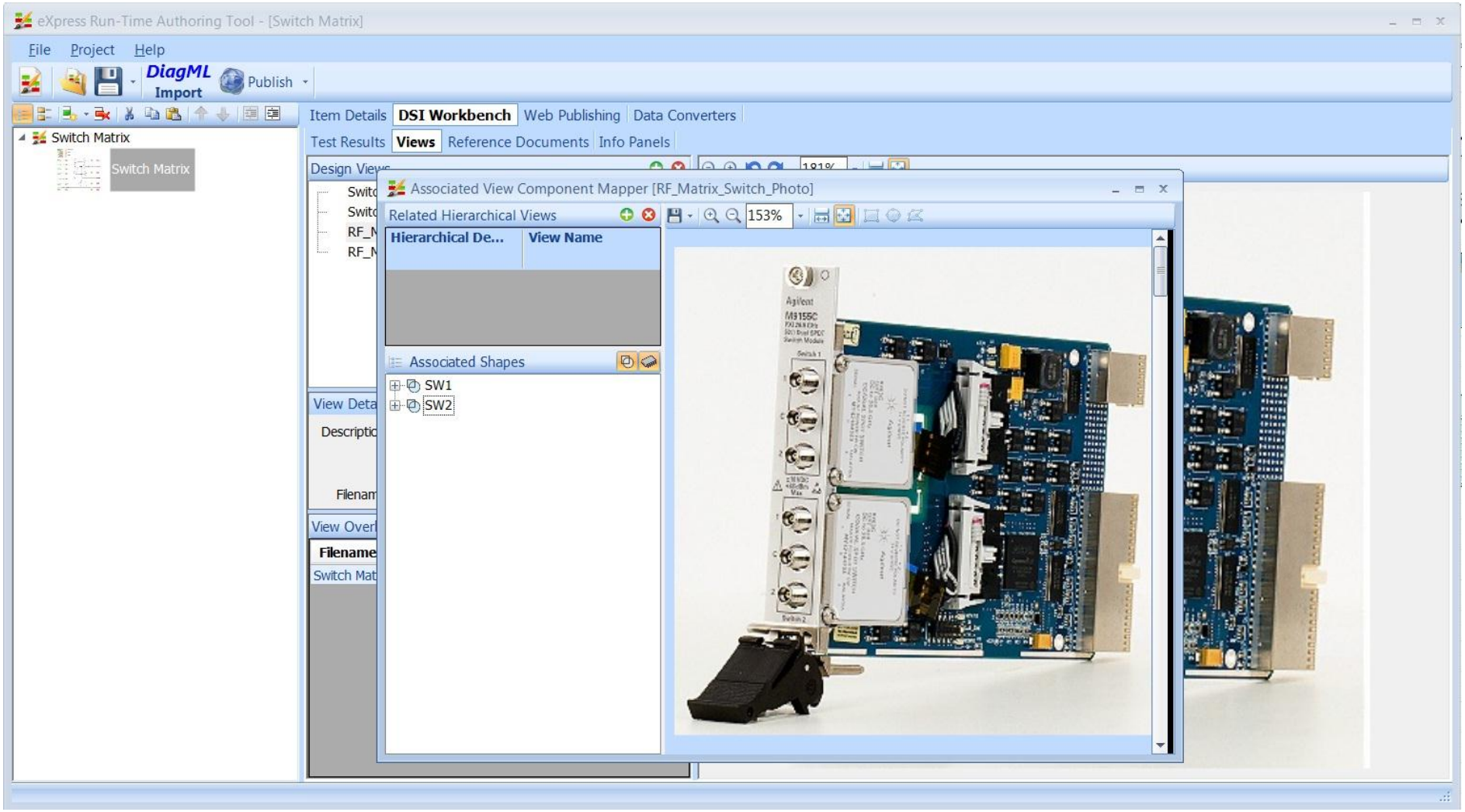
DiagML Implementation (Test)



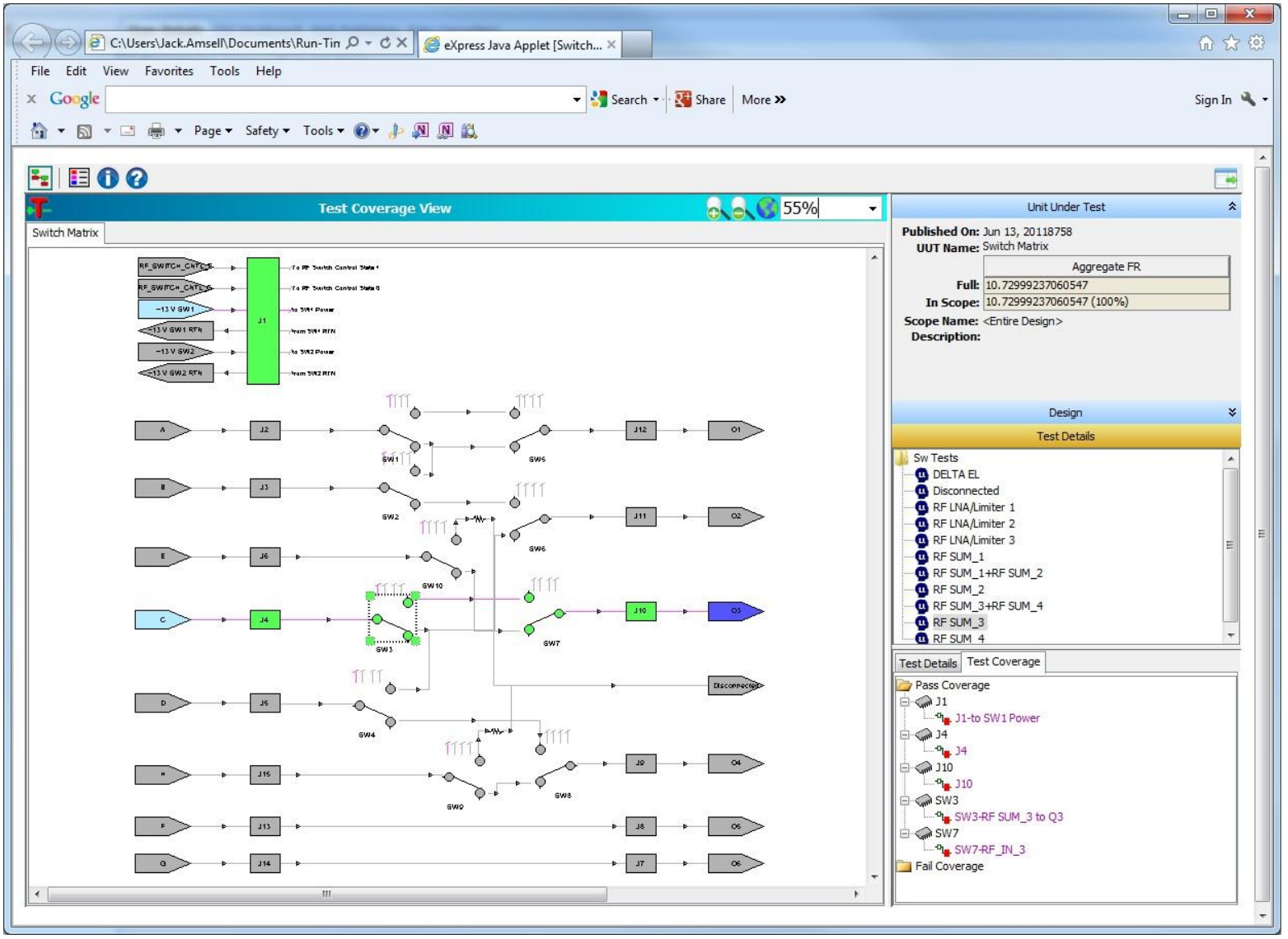
DiagML Implementation (Diagnostics)



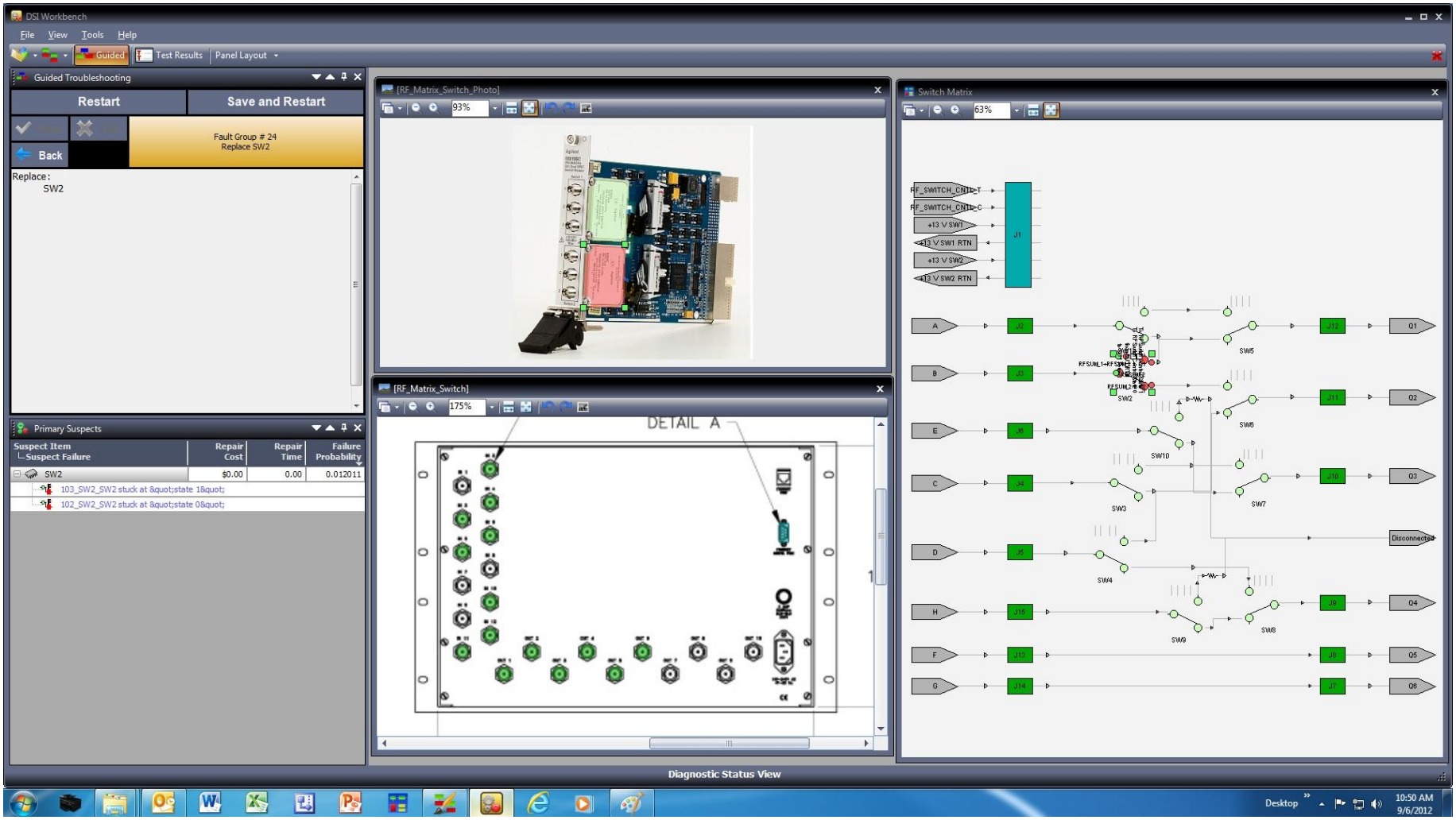
Merging Diagnostics to Resources



Using RTAT Java Applet to Share



Using All Resources in Test Environment

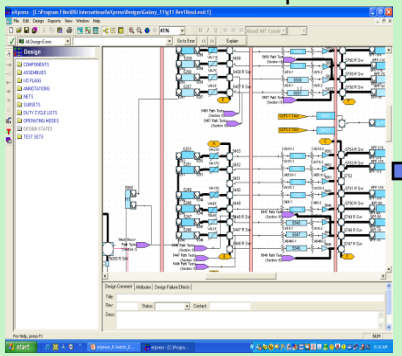


Towards Design-to-Test (DTT) Methodology

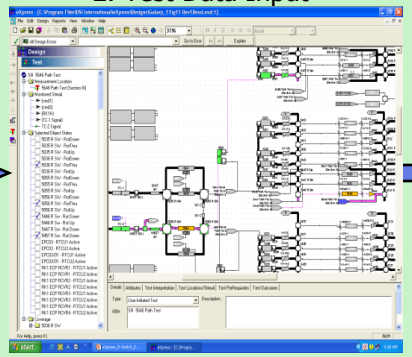
The Vision: Design-to-Test (DTT)

System Engineering Environment

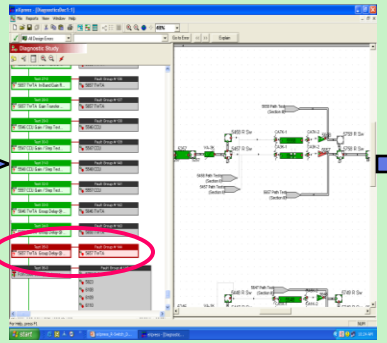
1. UUT Model Input



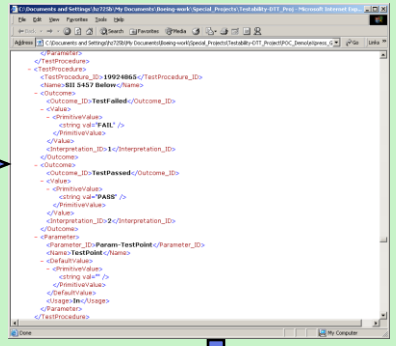
2. Test Data Input



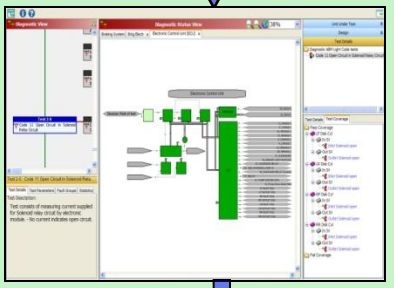
3. Test Strategy Generation



4. DiagML Export

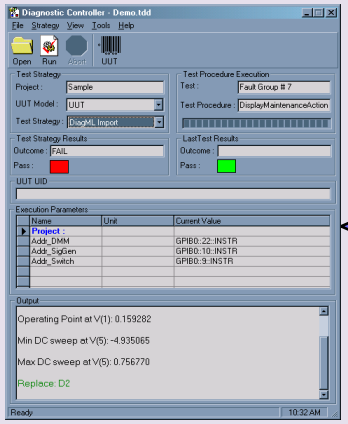


5. RTAT Formats Test Strategy Export

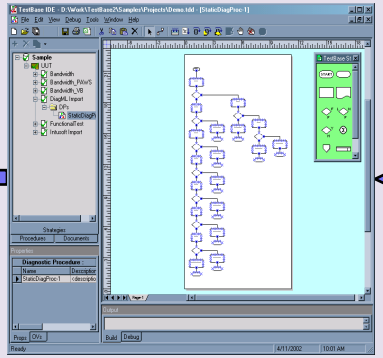


Test Engineering Environment

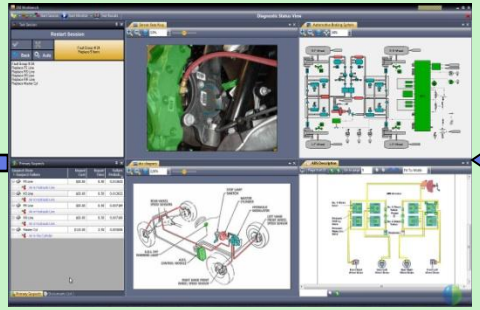
6. Test Strategy Execution



7. Test Exec Links Diagnostic Strategy to Test Procedures



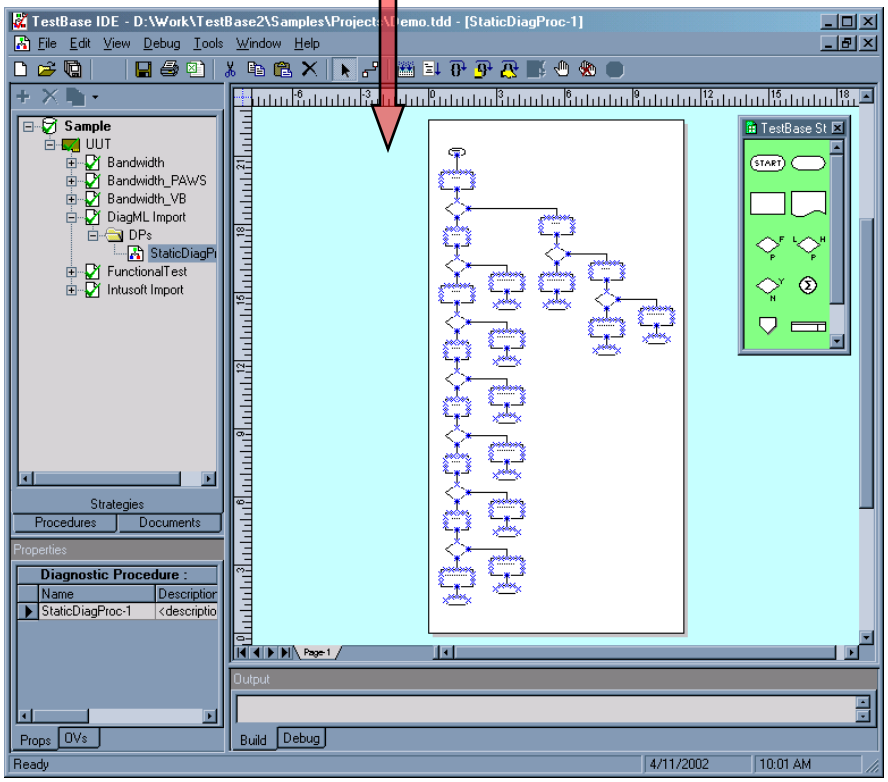
6. Workbench Preps for Test Exec

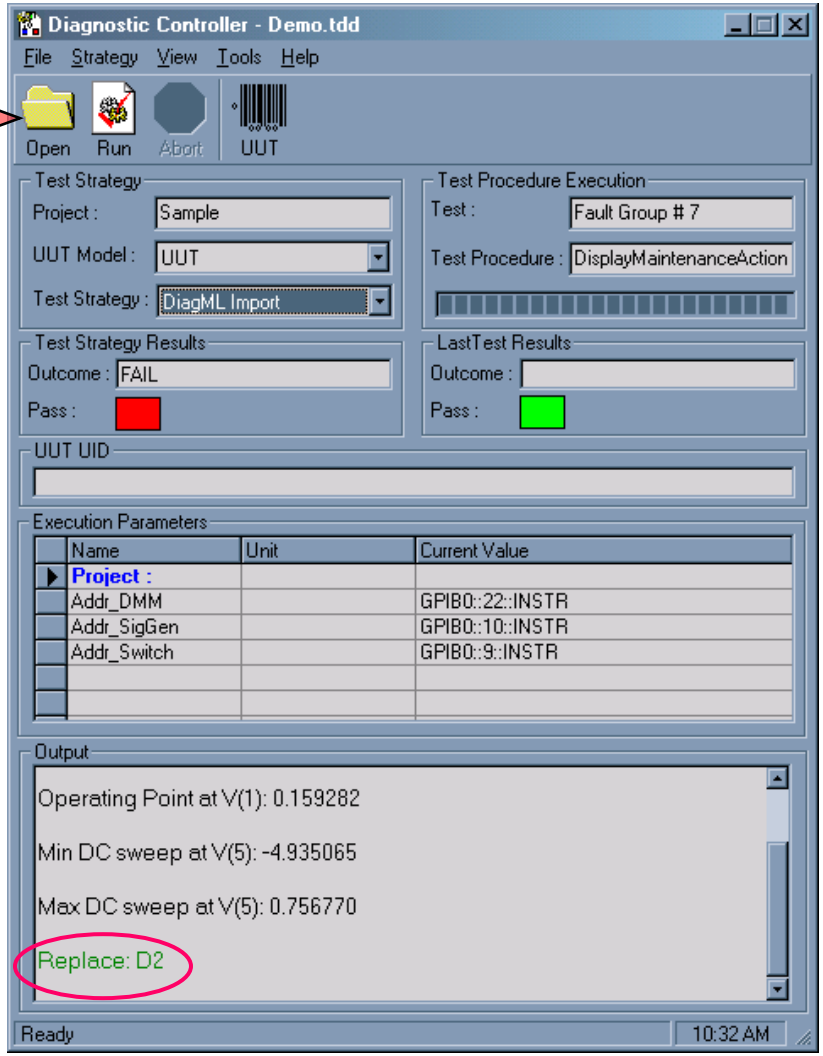


“Test Vectors” Used for Dynamic Testing

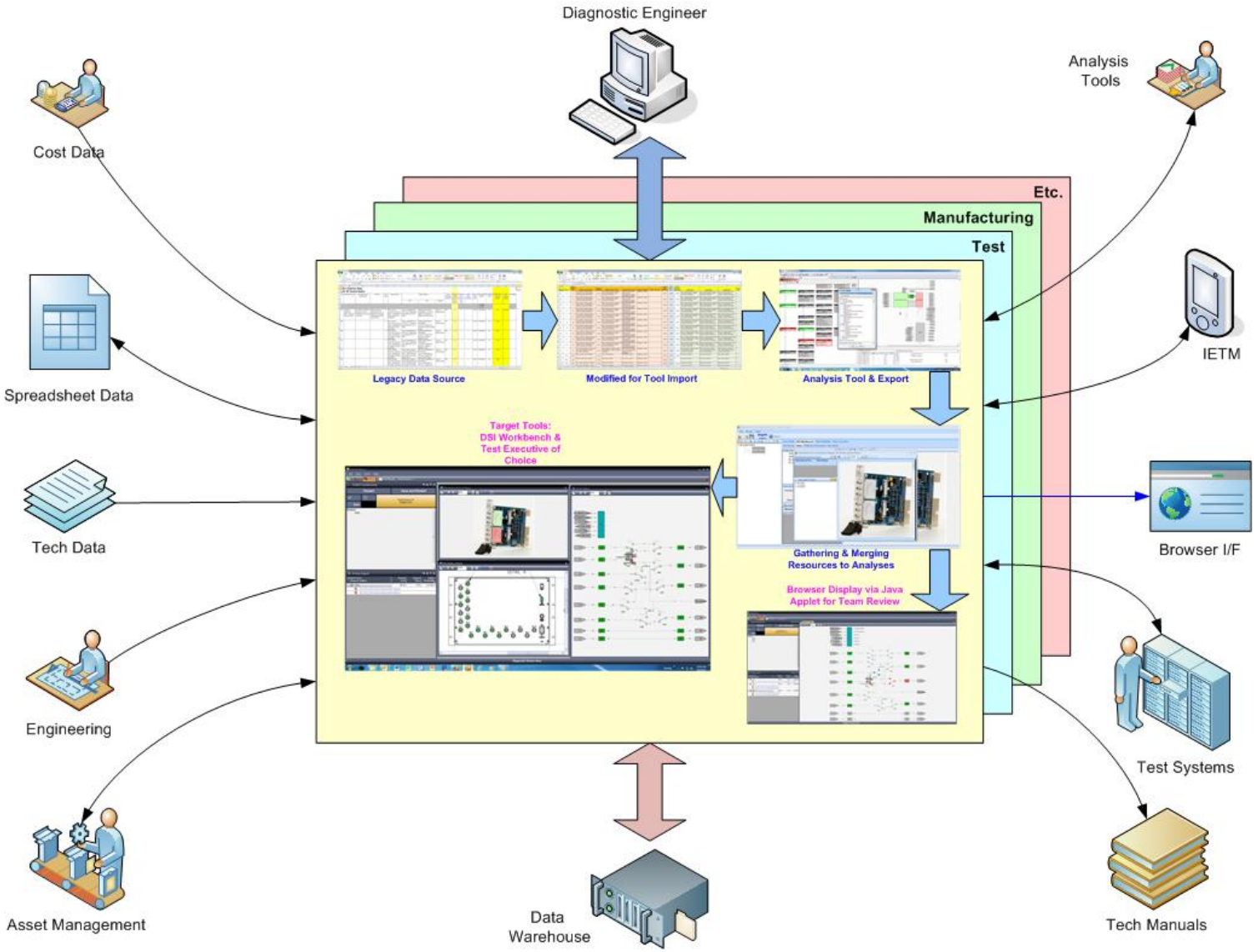
B) Test Strategy Execution

A) Test Strategy Import in TestBase





Integrated Diagnostics in the Enterprise



Wrapping it up

- **Historical**
  - **Hi-tech companies needed to identify, quantify, and analyze products for deployment and support**
  - **Tools and processes were developed for different "ilities" to address those needs**
- **Integrating and "Leaning" of Processes**
  - **Functional areas needed to be interconnected and streamlined to enhance productivity goals**
  - **Tools needed to be developed to facilitate process integration without compromising efficiencies or quality**
- **Today's Economic Challenges**
  - **Economic adversity has become a "deal breaker" for companies trying to compete for business, especially in defense procurements, by using legacy approaches**
  - **The ISDD approach leading to DTT directly addresses the aforementioned challenges today and into the future**
  - **It will become a critical competitive advantage for suppliers to shift their paradigm from just checking off a requirement to that of proactively enhancing their offerings to meet the demands of budget constraints while offering high quality performance**